

# Application Note AN-2009

## Using the FMS7401 to Implement a 200KHz Full-Digital Dimming Ballast for a Fluorescent Lamp

### Abstract

This application note describes how to use the FMS7401 Digital Power Controller (DPC) to digitally implement a power compact fluorescent lamp ballast with a power range of 32–57W. The FMS7401 is designed to have a variable frequency output pulse, such as Pulse Frequency Modulation, (PFM), of 8- or 12-Bits resolution, as well as a typical microcontroller feature including a sampled 8-bit A/D converter with an internal programmable memory. The variable frequency is used for driving the series-resonant network with a fluorescent lamp. By changing the driving frequency, the lamp can be preheated for accurate pre-heating time. For protection purposes, the lamp current is monitored and can be controlled through a closed current loop. The DPC can also identify any fault conditions such as over-voltage, over-current, over-heat, strike fail, or broken filament. Based on the programmable feature of the FMS7401, a highly-intelligent ballast can be realized. A 32W full-digital ballast is designed for a power compact fluorescent lamp from GE lighting with a running frequency of 180KHz for maximum power and a pre-heating frequency of 400KHz so as to reduce a bulky series inductor. The experimental results are provided.

### Introduction

Typically, analog ballasts have many external capacitors and resistors to control various parameters, such as pre-heating time, soft-start time, minimum and maximum driving frequencies, and running frequency. Those passive components may have a value deviation. Furthermore, the passive component values may vary with temperature variations. For a dimming feature, an analog-based controller needs an analog external signal. Therefore, external microcontrollers or microprocessors must be used in order to send the analog dimming signal through the D/A converter. Hence a simple, low-cost, fully-digital-based ballast is needed to provide more intelligent features such as identifying various lamps by monitoring an ignition voltage, lamp removal, recognition of end of lamp life, optimized pre-heating time setting, and so on.

This application note introduces a dedicated digital ballast controller, the FMS7401, which is designed for a closed current/voltage control feature to maintain a constant illumination. Additionally, the FMS7401 can update internal parameters by modifying data into EEPROM while driving a lamp. The FMS7401 has an internal RAM of 64-byte, a EEPROM of 64-byte, and a programmable EEPROM of 1-Kbyte with a 4-channel 8-bit A/D converter. The FMS7401

has fast Pulse-Width-Modulation (PWM) or Pulse-Density-Modulation (PFM) functions based on digital hardware structure including all conventional microcontroller features, such as EEPROM, RAM, A/D converter, and programmable voltage reference. There are also OP-Amp and analog comparators for fast control purposes. Internal PLL is also provided so that the frequency of the internal digital PWM block can be increased up to 64MHz, which can be an 8-bit resolution with a 250KHz PWM frequency.

In this application note, a full-digital ballast with a 180KHz running frequency and a 400KHz pre-heating frequency is designed in order to use a small inductor and pre-heating capacitor. A design guideline with initializing internal registers and main software structures will be described in detail.

### Ballast System Design

The resonant passive components  $C = 1.5\text{nF}$  and  $L = 330\mu\text{H}$  and the pre-heating and running curves are shown in Figure 4. The natural resonant frequency is  $f_{rc} = 226\text{KHz}$ . Hence, the required driving frequency range is in the 180–400KHz range. A DC link voltage is obtained by rectifying a voltage doubler output as shown in the complete schematic diagram in Figure 5. If  $V_{ac} = 110$ , then the DC link voltage becomes about  $300V_{dc}$ . The power rating of the target compact lamp is 32W, Biax T/E from GE lighting. A system efficiency of about 90% is expected and the input required power becomes 36W. Based on these parameters, a detailed explanation on how to set the control registers of the FMS7401 to drive the lamp properly will be given.

### Setting the System Clock

Figure 1 shows the conceptual block diagram of the FMS7401's clocking circuit. An internal clock Fclk of FMS7401 is generally recommended to be set to  $F_{clk} = 2\text{MHz}$  which can be adjusted and tested by setting the initial register, INIT2, with Fairchild's Emulator/Simulator Tool kit. This Fclk is an input clock of the digital multiplier (or Phase-Locked-Loop: PLL). The multiplication factor of PLL can be adjusted from 4/8/16/32MHz by using a 2-Bit of FS[1:0], where FS[1:0] = PSCALE[6:5] and the enable input of PLEN = PSCALE[7]. If Fclk is set to 2MHz, the output of the digital multiplier can be 8/16/32/64MHz depending on FS[1:0]. The output of PLL goes to the digital switch input B as shown in Figure 1. The digital switch output Y can be 1MHz if FSEL = 0 or 8/16/32/64MHz if FSEL = 1, where FSEL = PSCALE[4]. The output of digital switch Y becomes  $F_{pwm}$ , which is a base clock of the internal digital PWM counter.

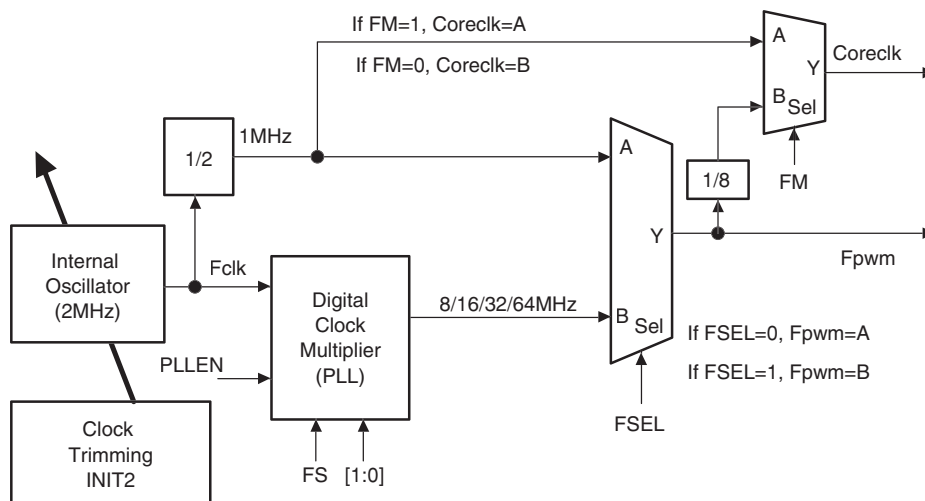


Figure 1. FMS7401 clock and PLL structure.

However, if FM is set to “1”, then Coreclk = 1MHz. Otherwise if FM is set to “0”, Coreclk = Fpwm/8, where FM = PSCALE[3], as shown in Table 1. The Coreclk is a base clock of software execution. A software instruction time becomes 1 $\mu$ s by setting FM = “1”. If PSCALE is set to #11010000b, the PWM clock frequency Fpwm becomes 32MHz. Hence the lowest output frequency becomes 125KHz. Based on this setting, a higher output driving frequency can be obtained by reducing the T1RAL register value as described in the next section.

### Setting the FMS7401 PWM Block

The internal PWM block of FMS7401 is shown in Figure 2. The Fpwm frequency is coming from the output of PLL as explained in the previous section. This Fpwm is divided by  $2^N$  through PS[2:0] = PSCALE[2:0] register. The output of the divider becomes a base clock of TIMER1. There is pre-load counter register T1RA and TIMER1 is a free running up-counter. TIMER1 is automatically reset

whenever the TIMER1 value equals T1RA. This means that the PWMed output frequency can be controlled by changing the T1RA value as necessary.

The dead time is a rest time of both high and low side MOSFETs. The high and low side MOSFETs, Q1 and Q2, should be simultaneously turned off during dead time. This dead time provides a complete turning off of both MOSFETs. If there is no dead time, then a current from the high side to low side MOSFETs can flow directly from the DC link. This current can cause useless switching losses as well as noise due to a large current spike. This dead time can be controlled by setting DTIME register.

There are two registers, T1CMPA and T1CMPB, for comparison purposes in order to provide the PWM output signal. If the TIMER1 count value exceeds the value of the T1CMPA, then the digital comparator output OA level becomes high as shown in Figure 3. This comparator output

### PSCALE

7	6	5	4	3	2	1	0
PLLEN	FS1	FS0	FSEL	FM	PS2	PS1	PS0

PLLEN = “1” → PLL enable, PLLEN = “0” → PLL disable.

FSEL = “1” → Fpwm = Fclk x 4 (FS = #00b), Fclk x 8 (FS = #01b), Fclk x 16 (FS = #10b), Fclk x 32 (FS = #11b)

FSEL = “0” → Fpwm = 1MHz if Fclk = 2MHz.

FM = “1” → Coreclk = Fclk/2 (FS = #00b), Fclk (FS = #01b), Fclk x 2 (FS = #10b), Fclk x 4 (FS = #11b) MHz.

FM = “0” → Core clock = Fclk/2

FS1	FS0	FM	Coreclk (MHz)	Fpwm (MHz)	PWM Freq. (8-bit) (KHz)
0	0	0	1	8	31.25
0	1	0	1	16	62.5
1	0	0	1	32	125
1	1	0	1	64	250
0	0	1	1	8	31.25
0	1	1	2	16	62.5
1	0	1	4	32	125
1	1	1	8	64	250

Table 1. Clock Control Register PSCALE of FMS7401

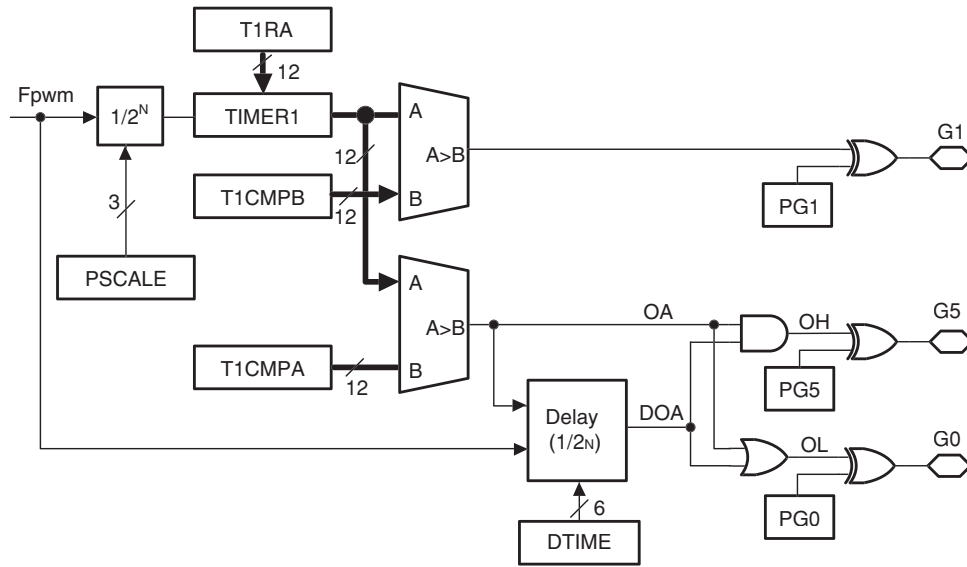


Figure 2. Conceptual Block Diagram of FMS7401's Digital PWM Structure.

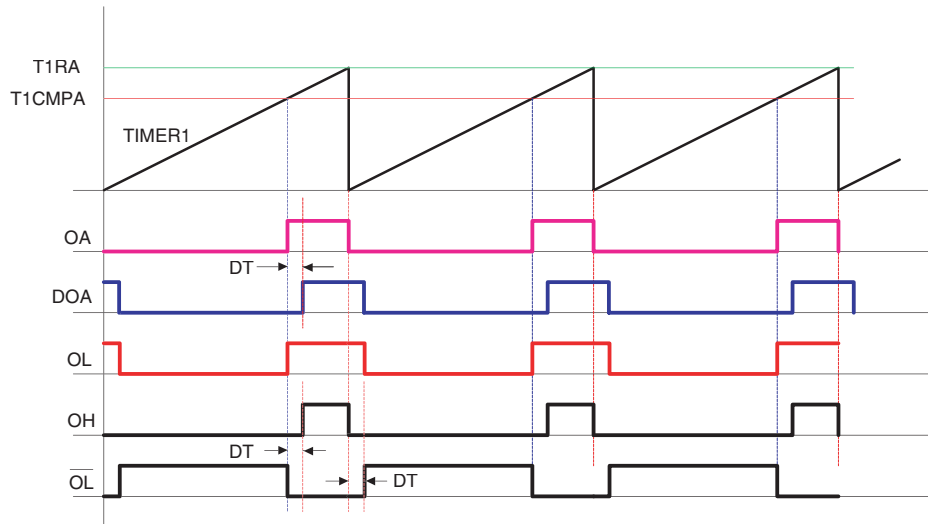


Figure 3. Key Waveforms of FMS7401's Digital PWM Block.

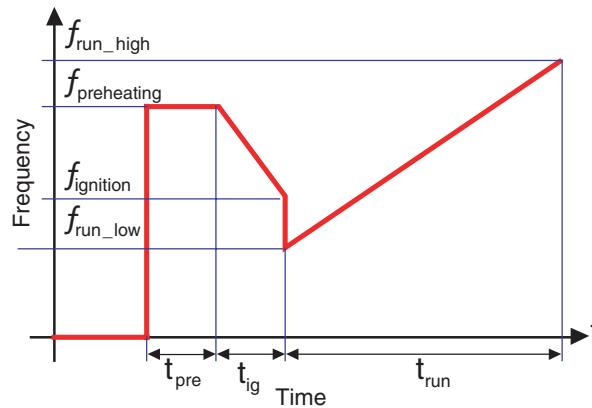


Figure 4. Digital Ballast Driving Frequencies.

OA level becomes an input of the OR gate and AND gate. The comparator output OA is delayed through Delay Block ( $1/2^N$ ) according to a 6-Bit DTIME setting value. This delayed output DOA becomes other inputs of the OR gate and AND gate as shown in Figure 2. Hence the outputs of the OR gate and AND gate, OL, and OH, become real high and low-side MOSFET gate signals.

Since a clock of delay block is coming from Fpwm, dead time can be adjusted from 0 to  $2^N$  of Fpwm clock of 32MHz ( $t_{pwm} = 31.25ns$ ) by using the 6-Bit DTIME register. Hence dead time can be controlled up to  $0-2\mu s$  ( $64 \times 31.25ns = 2.0\mu s$ ) with one step resolution of 31.25ns if Fpwm = 32MHz by setting PSCALE = 0xD0 (#11010000b).

Generally it is recommended to set a sufficient time because MOSFETs are switched on with zero-voltage switching condition. For example, if a low side MOSFET is turned off, the inductive current can immediately flow through the anti-parallel diode of the high-side MOSFET. Hence sufficient dead time is guaranteed as long as the anti-parallel body-diode is conducting.

In this application, 8-Bit resolution of 12-Bit TIMER1, T1RA, T1CMPA, and T1CMPB is used and DTIME is set to 3 for about  $t_{dead} = 0.1\mu s$ . As can be seen in the waveforms of OL and OH in Figure 3, the outputs are not proper for high and low sides MOSFETs' signals because both ON time intervals exist. Hence it is necessary to set PG0 to "1" in order to invert the digital comparator's output of OL level. This can be done by using the PORTGC and PORTGD registers. If one of bit PORTGC is set to "1", the set pin is defined as the output port. Otherwise, one of bit PORTGC is set to "0", the bit is defined as input pin. In this application, high and low side output signals should be defined as output pins.

As can be seen in Figure 3, the gate signals of OH and inverted OL properly provide a dead time defined in DTIME register for using MOSFET gate driving signals.

Setting requirements explained above can be programmed as:

```
LD PSCALE, #11010000b ; Fpwm = 32MHz, ts = 8μs
LD DTIME, #00000011b ; dead time is set to 0.1μs
LD PORTGC, #00100001b ; G5 and G0 are defined as output pins.
LD PORTGD, #00000001b ; PG0 = "1".
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### Ballast System Design Considerations

Lamp preheating can be started by driving two MOSFETs with the pre-heating frequency,  $f_{preheating}$ , during a preheating time,  $t_{pre}$ . The pre-heating time can be realized by

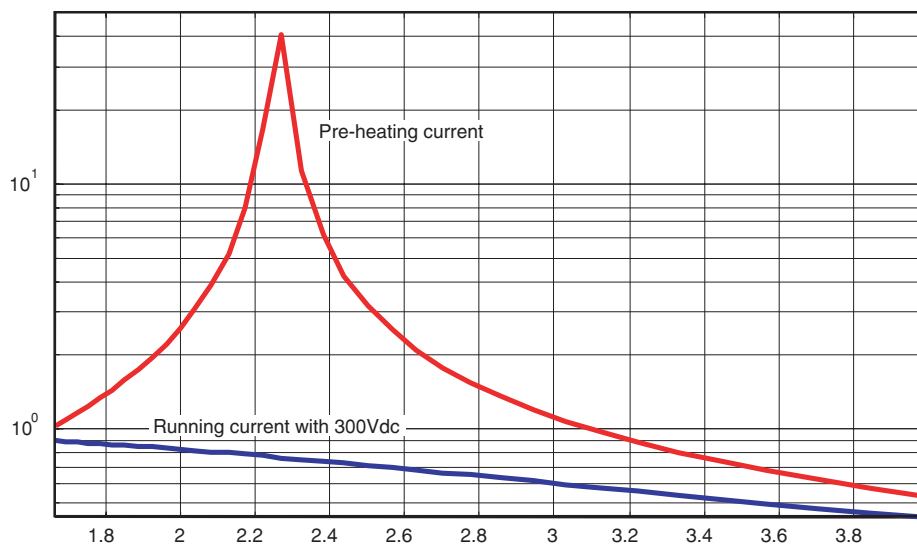
providing a wait loop for the pre-heating time,  $t_{pre}$  without any external passive components. The pre-heating time is also programmable for various lamps that require a different pre-heating time. Depending on the lamp power rating, the running frequency can be adjusted by changing the T1RA value.

At this high frequency, a resonant capacitor across the lamp has low impedance. The lamp does not ignite because of the low voltage drop. As the lamp filaments heat up, the driving frequency is lowered to the ignition frequency,  $f_{ignition}$ , linearly according to the programmed sequence with an ignition time,  $t_{ig}$ . If the lamp is ignited, then the driving frequency is reduced to a running frequency,  $f_{run\_low}$ , for maximum illumination. Now the dimming mode can be started by controlling the driving frequency from  $f_{run\_low}$  to  $f_{run\_high}$ .

The external resonant components of L and C are selected to have a high driving frequency so that the passive components size should be small. The resonant components of L = 330μH, 2A from Coilcraft and C = 1.5nF, 630V are used. Therefore, the resonant frequency becomes 226KHz. The target lamp is a 32W power compact lamp of Biax T/E from GE. This lamp voltage and current rating is 100V, 0.32A, and  $f > 20KHz$  and a 2-second preheating time are recommended. Details for this lamp are shown in reference [2] at the end of this application note.

First the FMS7401 turns off both high and low side MOSFETs in standby mode. There is no power supplied to the lamp and no power dissipation. This feature can eliminate a bulky mechanical main-power switch. Before the lamp is ignited, it has a high impedance. Hence the circuit forms a typical series resonant circuit with L and C.

If a pre-heating frequency is started above the resonant frequency, then  $t_{preheating}$  is set to  $2.5\mu s$  ( $f_{preheating} = 400KHz$ ). The voltage drop across the lamp is the same as the voltage across C as shown in Figure 5. The lamp has a high impedance before it is ignited. So the typical output network can be considered as an L-C series resonant circuit. Since lamp impedance is very high, the driving current is now flown through the half bridge  $\rightarrow L \rightarrow$  lamp filament  $\rightarrow C \rightarrow$  lamp filament  $\rightarrow$  DC link. Hence, both sides of the lamp are heated. The pre-heating time is set by using a wait loop in the software routine. After waiting for the required pre-heating time, the driving frequency is decreased by increasing the T1RA value in the software routine. As the driving frequency is reduced, the lamp voltage increases to close to the ignition voltage level.



**Figure 5. Pre-Heating and Running Curve of Resonant Circuit with  $L = 330\mu\text{H}$  and  $C = 1.5\text{nF}$ . (The x-axis is the driving frequency in 100KHz.)**

If the lamp is ignited by a high voltage level, then the lamp impedance is suddenly decreased and current near inductor levels flows through lamp, not through C. At this time, the lamp current is well limited because of the series impedance of the inductor with running frequency. The driving voltage from the DC high voltage source is applied to the series inductor and lamp. Thus the driving output power or lamp voltage can be controlled by changing the running frequency since the voltage drop of the series inductor is proportional to its frequency.

The T1RA register is used for changing a driving frequency. The T1RA is set to:

#0x50 for  $t_{\text{preheating}} = 2.5\mu\text{s}$  ( $f_{\text{preheating}} = 400\text{KHz}$ ),  
 #0x82 for  $t_{\text{ignition}} = 4.06\mu\text{s}$  ( $f_{\text{ignition}} = 246\text{KHz}$ ),  
 #0x78 for  $t_{\text{run\_high}} = 3.75\mu\text{s}$  ( $f_{\text{run\_high}} = 267\text{KHz}$ ), and  
 #0xB4 for  $t_{\text{run\_low}} = 5.625\mu\text{s}$  ( $f_{\text{run\_low}} = 178\text{KHz}$ ).

## Experimental Results and Discussions

An experiment is carried out with a Biac 32W compact fluorescent lamp. A DC link voltage of 300Vdc is supplied from the voltage double rectifier. The input power is measured at the DC input side by using a power analyzer, PM3000A. A power device, IRF840B (500V, 8A) MOSFET from Fairchild Semiconductor is used. The passive resonant inductor and capacitor are 330nH and 1.5nF. A natural resonant frequency of 226KHz is obtained. Hence ignition frequency is set under 226KHz. The FMS7401's clock is set to 2MHz to have a frequency variation range of 125KHz to 500KHz. The dead time is set to 0.1 $\mu\text{s}$ .

Figures 6 and 7 show experimental results of SOA curves when pre-heating with 400KHz and running for maximum power with 178KHz, respectively. If the high side MOSFET is turned off, then the MOSFET drain current is commutated to the low side anti-parallel body diode. This means that the low side MOSFET drain voltage becomes zero before a gate signal is applied. Since MOSFETs are switched with Zero-Voltage-Switching (ZVS) condition, the switching frequency can be increased without causing additional switching losses. Experimental results showing this switching characteristic can be seen in Figures 6 and 7. The SOA trajectory is moved closed to the x-axis or y-axis when ON or OFF transition is changed. It indicates that MOSFETs are safely turning on with ZVS condition. Furthermore, the SOA curve shows that the MOSFET is well-guaranteed ZVS condition in pre-heating mode as well as running mode with full power lamp voltage.

The experimental result of programmed starting modes such as standby mode, pre-heating, ignition, and full running modes are obtained as shown in Figure 9. As can be seen, the MOSFETs are switched on or off within the lowest voltage and current cross area. Hence very low switching losses are expected.

Figure 8 shows a voltage across the lamp and lamp current as programmed operation. A position **A** indicates MOSFET turn-off while DC link voltage, 300Vdc, is alive. The lamp current is interrupted, since the MOSFET's high and low sides are turned off. The lamp voltage after **A** is an imaginary voltage because both MOSFETs are turned off. So a lamp circuit becomes an open-circuit. Therefore the apparent voltage between **A** and **B** is practically zero. A pre-heating mode starts at **B**. The lamp current is kept at zero because all driving current flows through the series inductor,

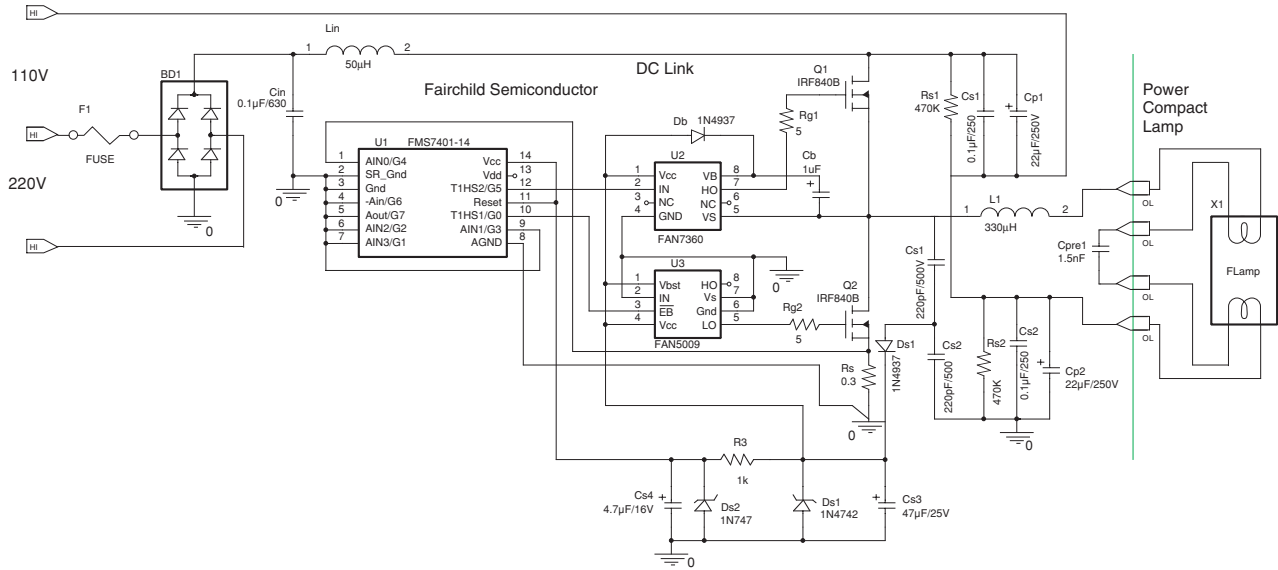


Figure 6. Overall Circuit of Full Digital Ballast using the FMS7401.

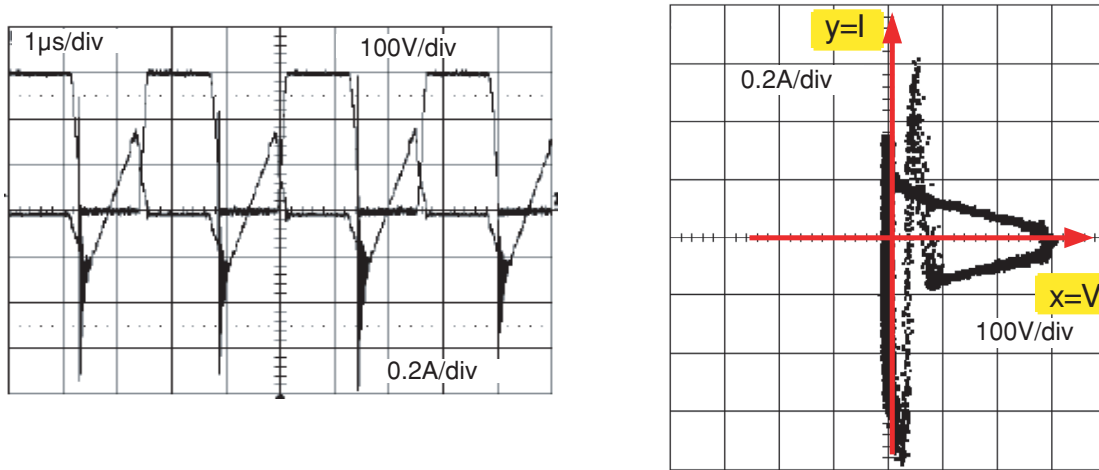


Figure 7. MOSFET's SOA Curve During Pre-Heating Mode.

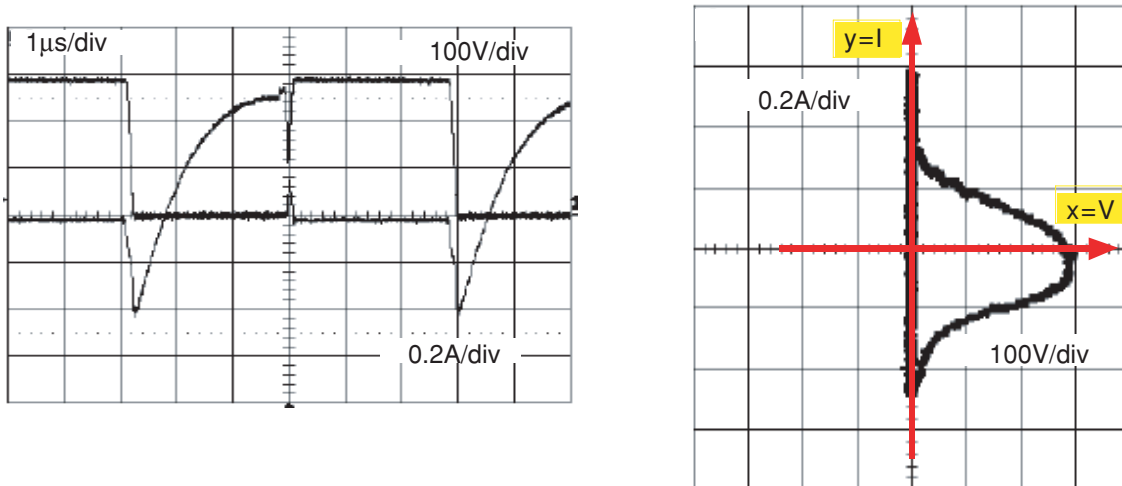


Figure 8. MOSFET's SOA Curve for Running Maximum Output Power.

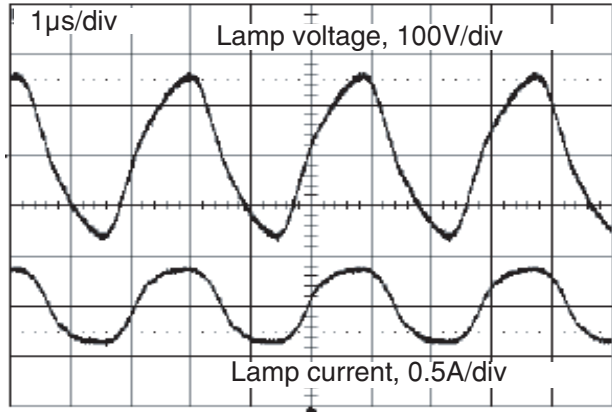


Figure 9. The Lamp Voltage Current Waveforms.

both side filaments of lamp, and the capacitor paralleled with the lamp. Hence filaments are heated with a pre-heating frequency of 400KHz.

An ignition mode is initiated at **C** by decreasing the driving frequency to 200KHz. If the driving frequency approaches the natural resonance frequency of  $f_{re} = 226\text{KHz}$ , the lamp voltage increases immediately. If this high resonated voltage exceeds the lamp ignition voltage, then the lamp is ignited and the lamp impedance becomes small. Hence the lamp current is increased from zero to a particular level depending on the ignition frequency at **C**. If the lamp driving power is still less than the rated power, then the lamp driving power can be increased by further reducing the driving frequency to the lowest frequency, where  $f_{run\_low} = 178\text{KHz}$  is for a Biax 32W power compact lamp from GE. The **D** shows an instance where the driving frequency is smoothly decreased from  $f_{ignition} = 246\text{KHz}$  to  $f_{run\_low} = 178\text{KHz}$ .

The MOSFET's output can be turned off by setting the FMS7401 port to be low, and then the lamp output is safely interrupted. To turn off the lamp more smoothly, the driving frequency should be increased with a slope so that the output power is smoothly decreased before the MOSFETs are turned off.

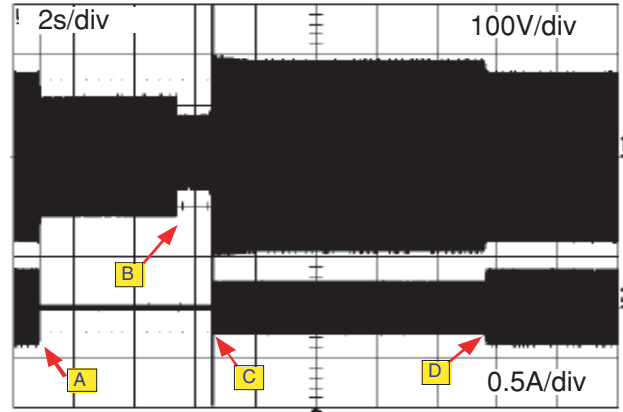


Figure 10. Programmed Operating Mode Results.

## Conclusion

The full digital control method and digital controller for electronic dimming ballast have been presented. The FMS7401 shows superior performance including a full dimming feature. Based on the FMS7401 with a programmed starting sequence, a more intelligent ballast can be designed. Typical fluorescent lamps such as F8T15/8W, F15T8/15W/18-inch, F32T8/32W, and F40T12/40W are also well-verified by using the FMS7401 with a high-driving frequency of 400KHz.

## Reference

1. FMS7401 data sheet at Fairchild web:  
<http://www.fairchildsemi.com/ds/FM/FMS7401.pdf>
2. The Biax T/E lamp data from GE lighting web at:  
[http://www.gelighting.com/na/downloadsbiax\\_te\\_32w\\_amgm.pdf](http://www.gelighting.com/na/downloadsbiax_te_32w_amgm.pdf).

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