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Fairchild Semiconductor
Application Note
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Guide to ALS and AS

Introduction

Since the introduction of the first bipolar Transistor-Transistor Logic (TTL) family (DM74), system designers have wanted more speed, less power consumption, or a combination of the two attributes. These requirements have spawned other logic families such as the DM74L (low power), DM74LS (low power Schottky), DM74S (Schottky), etc., in order to give the system designers some choice.

The most common way of comparing logic families is by using their speed-power products. Figure 1 displays a graphical representation of the logic families now available. The addition of the Advanced logic families broadens the spectrum of speed/power characteristics. This will allow the system designer to optimize his system's speed/power product by using performance budgeting. Performance budgeting is the intermixing of logic families to achieve the best speed/power product for a design. This is possible since bipolar logic families are designed to be fully compatible with each other. When the designer uses performance budgeting he is trading power consumption for speed. The designer identifies the speed critical paths and uses the fastest products to optimize the system's speed. For all other non-critical speed paths, the logic family with the best speed/power product should be used to optimize his system's power consumption. Since no other family offers the speed capability of AS and the low power of ALS, these families are the best choice when performance budgeting.

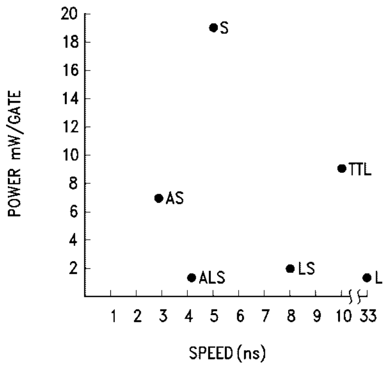

FIGURE 1. Speed Power Product Comparison

Each of the logic families is a compromise between speed and power consumption. Since the speed/power product is approximately a constant, a decrease in the power consumption must be traded off in a slowing down of the device and vice versa. The power consumption of a device is the easiest to control. By simply increasing the resistive values in the circuit the power consumption can be decreased.

The device speed can be handled in a similar manner. The speed of a device is limited by the charge stored in the transistors of the circuits. The time to remove this charge is proportional to the capacitance of the transistor and the current supplied. In the early speed improvements, the current aspect of this relationship was involved. A simple decrease in the resistive values in the circuits was done. This did help the speed but it greatly increased the power consumption. The advent of the Schottky transistor helped increase the device speed. The Schottky transistor adds a Schottky clamp diode between the base and collector of the transistor. The Schottky clamp diode has a lower forward voltage (about 0.4V) than the base-collector junction diode (about 0.5V). When the transistor is turned on the base current drives the transistor toward saturation and the collector voltage drops. This causes the Schottky clamp diode to conduct and divert some of the base current from the base-collector junction of the transistor. This clamp diode prevents the transistor from going into deep saturation. This allows the transistor to recover quickly by decreasing the transistor storage time. The Schottky logic families (DM74S, DM74LS) used the Schottky transistor and low values of resistors to achieve their high speeds.

Now Fairchild Semiconductor has introduced the Advanced Low Power Schottky (ALS) and the Advanced Schottky (AS) logic families. These families use a reduced transistor size, advanced process technology, and innovative design techniques to achieve the improved device speeds. This article will discuss various aspects of the Advanced logic families including design goals, application goals, circuit design enhancements, family features, and some helpful application tips.

Advanced Logic Families Design Goals

For the Advanced logic families our main design goal was to reduce the power consumption while improving the speed of the parts. We also set the requirement that the Advanced logic parts be pin for pin compatible with existing logic families to allow ease of system upgrading and interfacing with existing products.

The design goals for ALS family were to produce a complete logic family which would achieve one half the propagation delays of DM74LS at one half the power dissipation of DM74LS and improve the capability of the outputs to drive 50 to 100Ω lines.

For the AS family the design goal was to produce a complete logic family which would achieve one half the propagation delays of DM74S at one third the power dissipation of DM74S.

We set some goals for both Advanced logic families that were more application related because of our experience with other logic families. These goals were to improve the input characteristics and line driving capability, reduce internally generated supply current spikes, eliminate parasitic failure modes and decoding glitches, and provide better electro-static discharge protection.

An Overview of the Advanced Logic Families

The Advanced logic families (ALS & AS) have included most of the functions now present in the DM74LS and DM74S families. Some additions have been made to the Advanced families over the DM74LS and S families in order to make the families more complete. Both of the Advanced families have added a better (more complete) selection of octal bus transceivers, transparent latches and D-type flip-flops. A series of logic gate drivers (800 series) have been added to the ALS family. These devices have increased logic high and low current capabilities which allow the driving of high capacitive lines. These drivers have also been added to the AS family but have been designated the 1000 series. The ALS family has also added a series of gate buffers (1000 series) which increase the fanout of these devices by increasing the logic low and high driving capabilities (but not as much as the 800 series).

The datasheets for the Advanced Logic devices have been improved in order to more accurately reflect application requirements and to reduce the need for special testing. The supply voltage range for the commercial products has been defined as 10% (4.5V to 5.5V) instead of 5% as all other bipolar logic have done in the past. The high level output voltage specification has been changed to V_{CC}–2 to allow easier interfacing with CMOS parts which have V_{CC} sensitive thresholds and to better reflect the actual operation of the parts. The output drive current (I_O) is measured at a forcing voltage of 2.25V instead of 0V used by other logic families. This demonstrates that the Advanced logic families have sourcing capability through the threshold level of the next gate. The low level input current (I_{IL}) specification has been reduced from –400 µA used for DM74LS to –100 µA for ALS. This indicates that ALS devices' I_{IL} current is less of a dominant factor in the limiting of device fanout. Current sinking capability (I_{OL}) for the AS family of 3-STATE devices has been substantially increased (20 to 48 mA) over the DM74S family to allow the connection of these parts to a heavily loaded bus. The dynamic characteristics (propagation delays, etc.) have been specified over the supply voltage and temperature range. Also the output load used to test the dynamic characteristics has been simplified to allow easier construction of hardware for automatic test equipment and still reflect in-circuit operation. These items should give the designer a higher confidence level of the product used in his systems. Table 1 shows a comparison between ALS/AS and LS/S product. Appendix A includes generic datasheets for ALS and AS family of products.

TABLE 1. Family Comparison

Logic Family	Typical Delay (ns)	Typical Power (mW)	I_{OL} Max (mA)	I_{IL} Max (mA)
LS STD	8	2	8	–0.4
LS 3-STATE	8	6	24	–0.4
HC	8	—	4	–0.001
ALS STD	4	1.3	8	–0.1
ALS BUFFER	4	3	24	–0.1
74S	3	20	20	–2.0
AS	1.5	7.6	20	–0.5
AS BUFFER	2	8	48	–0.5

V_{CC} = 5V, C_L = 15 pF

Circuit Design Enhancements

One of the design enhancements of the Advanced logic families is the improvement of the input threshold voltage. Figure 4 (ALS schematic) and Figure 5 (AS schematic) are used for reference for the following discussion. The input threshold is determined by the following equation.

$$V_{threshold} = V_{BE(Q2)} + V_{BE(Q3)} + V_{BE(Q4)} - V_{BE(Q1)}$$

The typical VBE of these transistors is 0.7V. Therefore the typical threshold voltage is 1.4V. This optimizes the threshold point between the high and low level input voltages. This provides maximum noise immunity. Figure 2 demonstrates the threshold enhancement.

Another of the design enhancements is the use of a PNP transistor in the input circuitry. The use of the PNP transistor reduces the typical I_{IL} of these circuits (–10 µA for ALS and –50 µA for AS). When using a PNP transistor the equation for I_{IL} becomes:

$$I_{IL} = \frac{V_{CC} - V_{BE(Q1)} - V_I}{R(h_{FE(Q1)} + 1)}$$

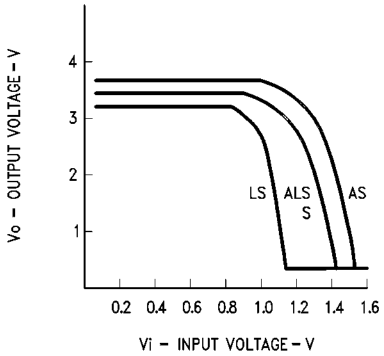

FIGURE 2. V_{IN} vs. V_{OUT}

Past logic families which used diodes or NPN transistors at the inputs had higher I_{IL} since they lacked the gain (h_{FE}) of the PNP transistor. The PNP transistor of the Advanced families effectively eliminates the I_{IL} current from being a dominant limiting factor in device fanout. The fanout constraints are now primarily associated with AC loading.

The input clamping and electrostatic discharge protection methods have also been improved. Past circuits have used diodes to do the negative voltage clamping action. The Advanced logic circuits use a Schottky transistor with the base and the emitter shorted to ground. The forward resistance of the base-collector is less than the diodes used in previous logic families. This lower resistance allows higher currents to be absorbed. This has improved the electrostatic discharge resistance from less than 1000V to 4000V. This gives the Advanced logic families a non-sensitive rating for the MIL-M-38510 people.

The lower output characteristic has been improved by the addition of the transistor (Q9) for the AS parts and the diode (D3) for the ALS. These elements provide additional base drive for the lower output transistor (Q5) when the output transitions from a high to low state. Thus the transistor pair Q3 and Q5 acts as a darlington pair. The AS parts use a transistor instead of the diode because of the higher drive requirements. Figure 3 shows the Advanced families output characteristic compared to the old Schottky families. Note that the current sink capability of the AS family takes off at 1.5V while the DM74S family remains flat. The ALS graph shows a similar characteristic but the break point is 1.8V.

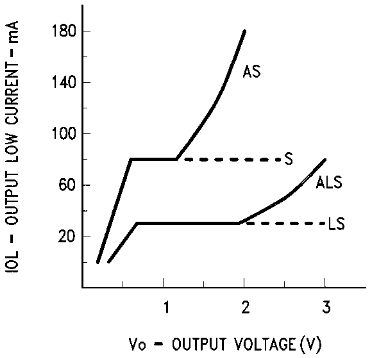

FIGURE 3. Low Logic Level V_{OUT} vs. I_{OUT}

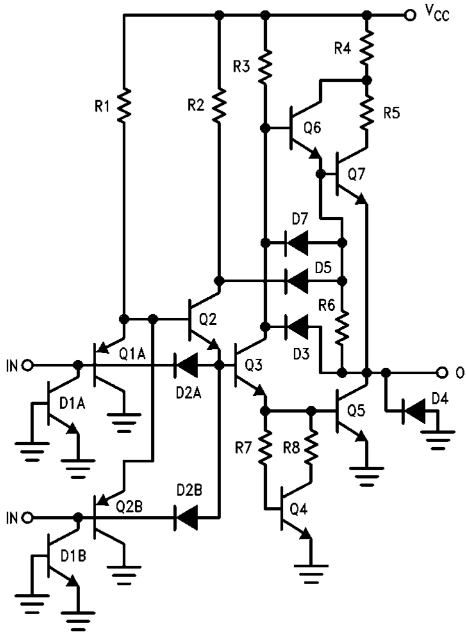

FIGURE 4. ALS00 Schematic

Circuit Design Enhancements (Continued)

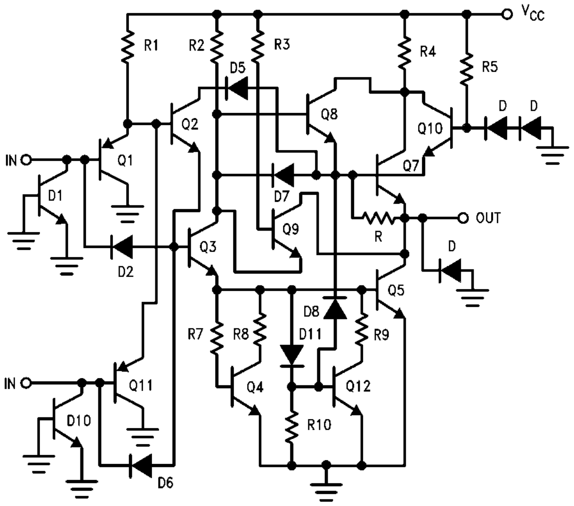

FIGURE 5. AS00 Schematic

The Advanced logic families include the output shaping circuit used in most modern bipolar logic families. This circuit consisting of transistor Q4, resistor R7 and resistor R8 helps to turn off the low output transistor Q5 during the low to high output transition. The diode D7 is used to help turn off the upper output transistor (Q7).

The AS circuits incorporate additional circuitry to reduce current supply spikes. During a LOW-to-HIGH transition a supply current spike can be produced because the lower output transistor (Q5) remains temporarily on. This can increase the power consumed by the circuit especially at high frequencies. The lower output transistor remains on because of charge being coupled by this transistor's base-collector capacitance. The circuitry used to eliminate this problem is the addition of a transistor (Q9), two diodes (D8 & D11), and two resistors (R9 & R10). This circuit has been named the Miller killer. The diode (D8) is used as a capacitor to couple charge into the base of the transistor, Q9, during a LOW-to-HIGH transition of the output. Thus Q9 turns on providing a means of turning off the lower output transistor (Q5). This circuitry is not required for most ALS devices due to the lower frequency of operation and smaller output structures.

Application Related Design Improvements

A major consideration in the layout of the Advanced logic families was their response to negative transients. The Advanced logic families have high transition rates which can generate large reflections (–2.5 volts) when terminated into a high impedance. A method of limiting reflections is to use a clamp diode. All the Advanced logic devices include Schottky clamp diodes on both the inputs and outputs. These clamp diodes may have to handle peak currents of 30 to 60 mA. At these currents substrate junctions will become forward biased.

Figure 6 shows a cross sectional view of the area of an Advanced logic device where a negative transient may be a problem. A negative transient on an input or output tank (the structure in the center) will forward bias the substrate to N epi junction. This will form a parasitic NPN transistor between adjacent structures. If the adjacent structure is an input or output the only impact will be an increase in the leakage current. Since most of the devices have an active totem pole output design a logic state change does not happen. If the adjacent structure is a collector of an internal transistor the increase in the leakage current may cause a logic state change from a high logic state to a low logic state. This state change in a combinational logic part can propagate to the output and cause a glitch which can affect the system performance. If the adjacent transistor is part of a flip-flop a change in the logic state can happen. This can cause a sequential error in the system.

Application Related Design Improvements (Continued)

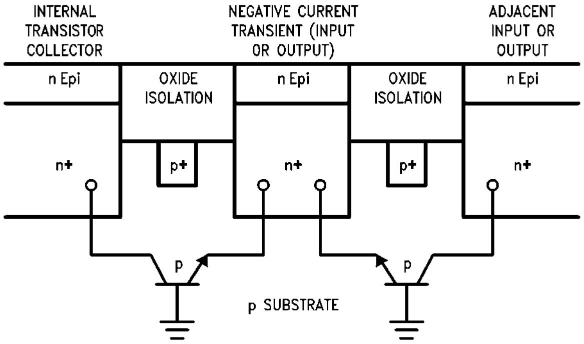

FIGURE 6. Parasitic Failures Modes

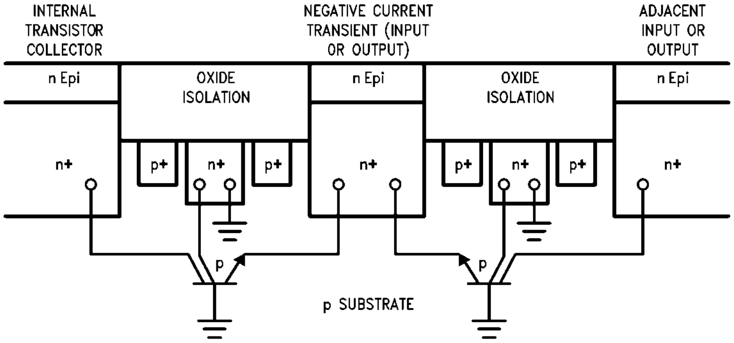

FIGURE 7. Solution to Parasitic Failures Modes

Figure 7 demonstrates the method we use to minimize this problem. A grounded N+ guard ring around all input and output transistors is included. The guard ring increases the spacing between the two structures thus reducing the efficiency of the parasitic transistor. The grounded guard ring also acts as an energy well which collects the majority of the electrons injected by the parasitic transistor. An example of the amount of protection achieved can be demonstrated by looking at the ALS74. Without the guard ring this device will change state with only −5 mA input current. With a guard ring the device can withstand in excess of −35 mA input current with no change in logic state and only a few tenths of a volt degradation of the high state logic level.

Another problem associated with older logic families is decoding glitches. The old method of decoding is demonstrated in Figure 8. A decoding glitch occurs when the A and B inputs are at a high logic level and the select input transitions from a LOW-to-HIGH logic level. The propagation delay from a high to a low logic level is faster for the inverting gate than the propagation delay from a LOW-to-HIGH logic level is for the non-inverting gate. This causes both the SEL and the SEL′ lines to be at a low logic level for a short time. If both these lines are at a low logic level at the same time the Y output will transition to a low logic level even if the A and B inputs are at a high logic level. With the circuit used for the Advanced logic families Figure 9 the SEL′ line cannot go to a low logic level until the SEL line goes to a high logic level since the SELECT and SEL lines are logically connected with a NAND gate.

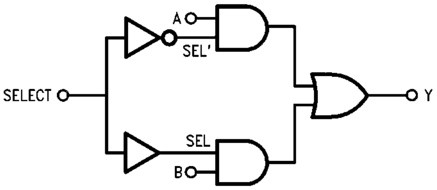

FIGURE 8. Old Method of Decoding

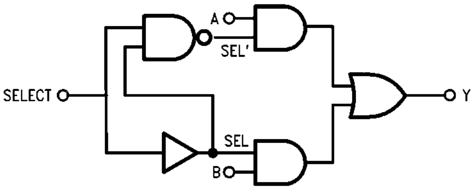

FIGURE 9. New Method of Decoding

Process Description

A major factor which allowed us to meet our design goals is the Advanced Schottky process. The Advanced Schottky process uses oxide isolation and ion implantation. This allows the physical size of the transistors to be reduced.

Figure 10 shows the size comparison between a junction isolated and oxide isolated transistors. The oxide isolated transistor is less than half the size of the junction isolated transistor. This reduction in size provides higher packing density and, most important, smaller active junction areas (2.5µ emitter width). The oxide isolated structure has much smaller capacitance due to the reduced geometries thus improving the speed/power performance (5 GHz f_t).

Figure 11 shows a cross sectional view comparison between the junction and oxide isolation processes. In the oxide isolated process the emitter of the transistor contacts the oxide isolation directly (walled emitter). This greatly reduces the side wall capacitance since the capacitance is inversely proportional to the dielectric constant and dielectric constant between silicon/oxide is much smaller than the dielectric constant between two sections of silicon.

Ion implantation is a technique of introducing impurities by bombarding the host material with a beam of ions. This technique is superior to the deposition method used in previous processes because it is easier to control the amount of impurities introduced into the silicon. The deposition method relies on control of diffusion time, diffusion temperature, gasflow rate and surface cleanliness. Ion implantation relies on the control of only current and voltage of the machine.

Figure 12 is a lengthwise cross sectional view of the oxide isolated transistor. From this figure it can be seen that the limiting factor of the size of the transistor is the metal interconnects and the spacing between the metal.

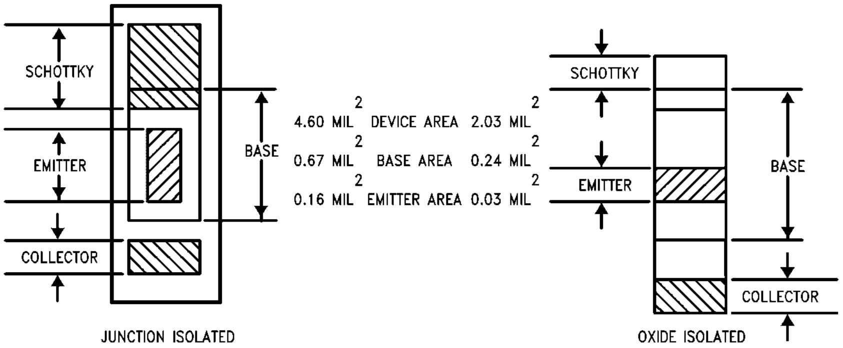

FIGURE 10. Top View of Junction and Oxide Isolated Transistors

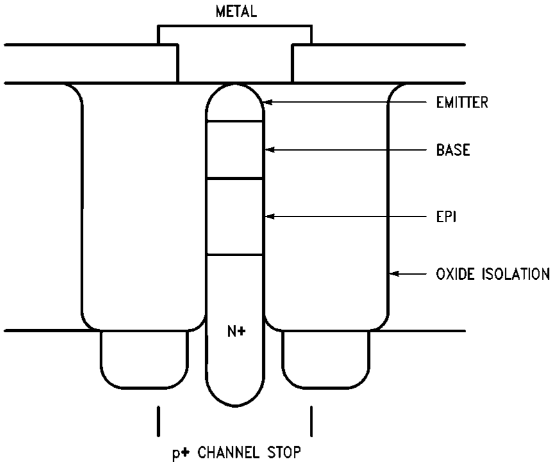

FIGURE 11. Cross Sectional View of Oxide Isolated Transistor

Process Description (Continued)

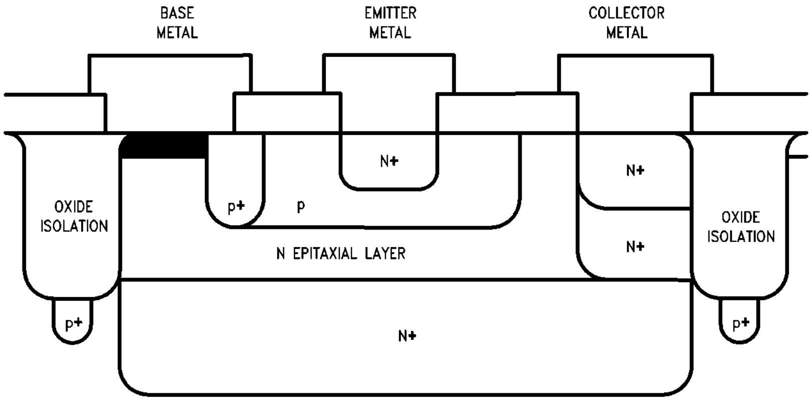

FIGURE 12. Cross Sectional View of Oxide Isolated Transistor

Noise Considerations

When a digital system is being designed, the designer works with a perfect mathematical system. Once the designer starts to layout his design he enters the real world where everything is not perfect. There are pitfalls in the laying out circuits that will make a perfectly good logic circuit work incorrectly and unpredictably. One of the major considerations in the layout of a circuit is noise. Noise is extraneous currents and voltages introduced into or produced by the circuit. When slower circuits are used consideration of noise is not as important as it is for fast circuits such as the Advanced Logic families. This is true because the slower circuits take longer to respond to noise and characteristically noise is pulses of short duration. The Advanced Logic families have addressed noise produced by the device itself, as mentioned previously, so it will not be addressed here. Noise can be introduced by several methods: external to the system, cross talk between lines, power supply spikes and line reflections. Each of these problems will be examined and solutions presented.

Noise Margin

Each logic family has a certain amount of noise margin. Noise margin is the voltage amplitude of an extraneous signal that can be added to the input level of a logic circuit before change in the output logic voltage level could occur. Worst case noise margin is defined as the difference between the minimum high voltage [V_{OH} (2.5V)] minus the maximum input high voltage [V_{IH} (2V)] or the maximum input low voltage [V_{IL} (0.8V)] minus the maximum output low voltage [V_{OL} (0.5V)] whichever is smaller. For the ALS and AS families these numbers turn out to be 0.5 and 0.3 volts respectively.

Power Supply Spikes

Power supply spikes can be introduced to the system externally or generated internally. As gates switch from one logic state to another, their current drain on the supply will change. The more gates that switch at the same time the greater the current drain on the supply will be. The speed of the changes is also a factor as will be demonstrated. These current changes produce voltage variations because of supply line resistance and inductance.

In most designs the supply lead inductance is the dominant factor. For a current change di in time dt with a lead inductance of L, the resulting noise voltage is defined as V = L[di/dt]. For a octal ALS buffer the current change can be 10 mA, the transition time can be 3 ns, and for a 15 cm line on a printed circuit board the inductance can be 0.1 µH. This will give a noise pulse of 333 mV. With several circuits switching at the same time this could produce a problem.

The solution to the problem is to include several decoupling capacitors evenly distributed around the board. Ceramic disc capacitors of 0.01 µF are often used. If a 0.01 µF capacitor is used in the above example the noise pulse would be greatly reduced. For a capacitor C and a current change di in the time dt the voltage change is represented by V = [(di) (dt)]/C. This gives a noise pulse of 3 mV. Usually one capacitor for every five ICs is sufficient. If more high power ICs (buffers and line drivers) are used a one to one ratio of capacitor to ICs might be required. Since the transition time of AS devices is so fast, each IC should have a bypass capacitor. These capacitors are inexpensive and will greatly increase the reliability of your design.

Line Reflections

Line reflection is another source of noise. Line reflection is caused by a difference in the impedance of the transmission line and the resistance of the line load. Each transmission line has a characteristic impedance which is the initial resistance seen by a signal entering the line.

Let's consider a simple circuit which includes a voltage source, a switch, a transmission line and a resistive load. The characteristic impedance of the transmission line is Z_0 and the resistive load is R. The resistive load, R, can be referred to as the terminating resistance. When the switch is closed the initial current flowing into the line will be $I = V/Z_0$. A current step of magnitude I and voltage step of V flows down the transmission line. The current required by

Line Reflections (Continued)

the load at the end of the transmission line is V/R. If the characteristics impedance of the transmission line does not equal the load resistance a partial reflection of the signal will occur.

One can define a reflection coefficient (Rho) as the reflected voltage amplitude divided by the incident voltage amplitude. It can be mathematically shown that the Rho = $[R - Z_0]/[R + Z_0]$. If R equals 0 (short circuit) the Rho equals −1. If R equals infinity (open circuit) the Rho equals 1. If R = Z_0 the Rho equals 0 which indicates that there will be no reflection. The magnitude of the voltage at the load resistance is initially V(1 + Rho). If a reflection initially occurs, further reflections will occur until I = V/R. Possible waveforms are shown in Figure 13.

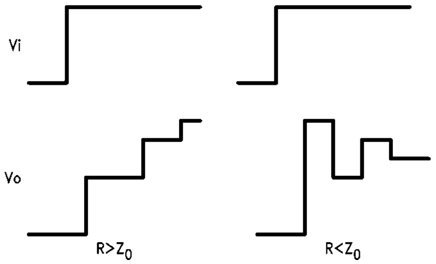

FIGURE 13. Waveforms for Improperly Terminated Transmission Lines

It can be shown that the duration of each reflection is equal to twice the time it takes for the signal to propagate down the transmission line. Generally, gates do not respond to a signal that is shorter than the propagation delay of device itself. A good rule of thumb to use to determine if a transmission line requires termination is if the time required for the signal to propagate down the transmission line is greater than one quarter of the propagation delay of the device the line should be terminated.

Let's calculated the maximum line length for some Advanced Logic family devices. Let's assume that the signal travels down the line at the speed of light (3 X 10 to the eight m/s). The maximum line length is the speed of light times one quarter the propagation delay of the device. The propagation delay of an ALS gate is about 4 ns. This would give a safe maximum length of the line of 0.3m (about 1 ft.). The propagation delay of an AS gate is about 2 ns. This would give a safe maximum length of the line of 0.15m (about 0.5 ft.).

Another method of termination of a transmission line is a series termination. It can be shown that the initial step received at an open circuit termination is twice the input step. If we have a series resistor at the transmitter that is equal to the characteristic impedance of the line the reflection would be absorbed by the series resistance. This method requires a high impedance receiver but uses less power than the previous method.

Cross Talk

Cross talk is the coupling of a signal from one line to an adjacent line. It is caused by the mutual inductance and capacitance between signal lines. Long parallel lines are the most susceptible to this problem. To minimize the effects of cross talk, proper shielding, grounding and decoupling should be done. On lines which may be particularly sensitive to cross talk, the distance between these lines should be increased.

Use flat cable with alternate signal/ground wires, coaxial cable, signal lines (PCB track) above ground plane with the minimum distance between lines equal to the distance between ground plane and signal plane, or twisted pairs to minimize cross talk.

Unused Inputs

Unused inputs which are left open circuited can be a source of noise. An open circuited input settles at the threshold voltage of that node. It can act as an antenna and accept a signal. To avoid this problem any unused input should be tied to a potential that will not cause a logic error. For example, unused inputs of AND gates, NAND gates, and active low presets and clears of flip-flops should be tied to a high potential. Unused inputs of NOR gates should be tied to ground. Unused inputs that are tied to a high potential can be connected directly to the supply voltage as long as the 5.5V maximum is not exceeded. A better method is to connect unused inputs to a high potential through a resistor (1 kΩ or greater) to the supply voltage. This will give some protection in case this input is shorted to ground. Several inputs can be connected to this resistor.

Open-Collector Outputs

All open collector outputs, whether used alone or in a wired-OR configuration, requires an external pull-up resistor. The resistor value is dependent upon the fanout of the OR tie and the number of devices in the OR tie. R(min) is determined so that if only one output is LOW the maximum allowable OR tie fanout is not surpassed. The R(max) value is calculated with all the OR tied outputs HIGH to sustain the necessary V_{OH}.

N = Number of Wired-OR Outputs

$$R_{(min)} = \frac{V_{CC(max)} - V_{OL}}{I_{OL} - M \times I_{IL}}$$

$$R_{(max)} = \frac{V_{CC(min)} - V_{OH}}{N \times I_{OH} + M \times I_{IH}}$$

M = Number of Inputs Being Driven

I_{IL} = LOW Level Input Current

I_{IH} = HIGH Level Input Current

V_{OL} = Output LOW Voltage (0.5V)

V_{OH} = Output HIGH Voltage (2.5)

I_{OL} = LOW Level Fanout Current

I_{OH} = I_{CEX} = Output HIGH Current

Open-Collector Outputs (Continued)

Example: Two ALS03 gate outputs driving three LS gates.

$$R_{(min)} = \frac{5.25V - 0.5V}{8\ mA - 3 \times 0.4\ mA} = 698\Omega$$

$$R_{(max)} = \frac{4.75V - 2.5V}{2 \times 0.1\ mA + 3 \times 0.02\ mA} = 16\ k\Omega$$

The R range for the pull-up is between 698 and 16 kΩ. The lower resistor values will provide faster speeds while the higher resistances give lower power dissipation.

Summary of AS/ALS Features

- Pin compatible with other 5V bipolar families
- Faster propagation delays
- Lower power consumption
- Better selection of octal bus transceivers, transparent latches, and D-type flip-flops
- Addition of series of line drivers
- Addition of series of buffers
- Dynamic characteristics specified over supply voltage and temperature range
- Improved input threshold voltage
- Improved ESD protection
- Better pin-to-pin isolation
- Elimination of decoding glitches

Appendix

Recommended Operating Conditions Advanced Low Power Schottky

Symbol	Parameter	Standard Output		Buffer Output		Bus Driver Output		Units
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	2		2		2		V
V_{IL}	Low Level Output Voltage		0.8		0.8		0.8	V
I_{OH}	High Level Output Current		–0.4		–2.6		–15	mA
V_{OH} (Note 1)	High Level Output Voltage		5.5		5.5		5.5	V
I_{OL}	Low Level Output Current		8		24		24	mA
T_A	Operating Free-Air Temperature	0	70	0	70	0	70	°C

Note 1: For open-collector outputs.

Electrical Characteristics Advanced Low Power Schottky

Symbol	Parameter	Conditions	Standard Output		Buffer Output		Bus Driver Output		Units
			Min	Max	Min	Max	Min	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = – 18 mA		–1.5		–1.5		–1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = Max			2.4		2		V
		V_{CC} = 4.5V I_{OH} = –3 mA					2.4		
		V_{CC} = 4.5V to 5.5V I_{OH} = –0.4 mA	V_{CC}–2		V_{CC}–2		V_{CC}–2		
I_{OH}	High Level Output Current	V_{CC} = 4.5V V_{OH} = 5.5V		0.1		0.1		0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = Max		0.5		0.5		0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V		0.1		0.1		0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V		20		20		20	µA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_I = 0.4V		–0.1		–0.1		–0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V	–30	–112	–30	–112	–30	–112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V				20		20	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, I/O Ports				0.1		0.1	mA
		V_O = 0.4V, Non I/O				–20		–20	µA
I_{CC}	Supply Current	V_{CC} = 5.5V							mA

Recommended Operating Conditions Advanced Schottky

Symbol	Parameter	Standard Output		Buffer Output		Bus Driver Output		Units
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	2		2		2		V
V_{IL}	Low Level Output Voltage		0.8		0.8		0.8	V
I_{OH}	High Level Output Current		–2		–15		–48	mA
V_{OH} (Note 2)	High Level Output Voltage		5.5		5.5		5.5	V
I_{OL}	Low Level Output Current		20		48		48	mA
T_A	Operating Free-Air Temperature	0	70	0	70	0	70	°C

Note 2: For open-collector parts.

Electrical Characteristics Advanced Schottky

Symbol	Parameter	Conditions	Standard Output		Buffer Output		Bus Driver Output		Units
			Min	Max	Min	Max	Min	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = –18 mA		–1.2		–1.2		–1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = Max			2.4		2		V
		V_{CC} = 4.5V to 5.5V I_{OH} = –2 mA	V_{CC}–2		V_{CC}–2		V_{CC}–2		
I_{OH}	High Level Output Current	V_{CC} = 4.5V V_{OH} = 5.5V		0.1		0.1		0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = Max		0.5		0.5		0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V		0.1		0.1		0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V		20		20		20	µA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_I = 0.4V		–0.5		–0.5		–0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V	–30	–112	–30	–112	–30	–112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V				50		50	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, I/O Ports				–0.5		–0.5	mA
		V_O = 0.4V, Non I/O				–50		–50	µA
I_{CC}	Supply Current	V_{CC} = 5.5V							mA