

## Design Innovations

# Address Advanced CMOS Logic Noise Considerations

### UNDERSTANDING THE FUNDAMENTALS OF NOISE

Today's electronic system designers are becoming increasingly more familiar with the issues involved in migrating to high-speed logic. One key issue is total system noise.

Noise in an electronic system can be described according to its source. The first category is system-generated noise, i.e., noise generated from the printed board up, such as power distribution and decoupling noise, crosstalk noise, electromagnetic interference (EMI), and transmission line reflections. System noise is a function of signal characteristics such as edge rate, voltage swing, and frequency. This type of noise can be minimized by strictly adhering to proper printed circuit board design practice commonplace in the design of ECL-based systems. The system designer can do more to control this type of noise than device-generated noise.

Device-generated noise is the second category, i.e., noise that is generated at the integrated circuit level such as simultaneous switching noise, or ground bounce, device undershoot, and dynamic input threshold shift. System designers may use techniques that minimize the level of device-generated noise. Device-generated noise is more effectively minimized by the IC designer and manufacturer. In some asynchronous applications, such as the distribution of timing signals, use of inherently lower-noise ICs can be critical.

### CONTROLLING

#### SYSTEM-GENERATED NOISE IS CRITICAL

The power distribution network is a key source of system noise. High-performance logic switches large amounts of current in a short amount of time and almost always requires multiple-plane printed circuit boards with separate power and ground planes instead of traces. Due to their high impedance, power and ground traces may generate too large of a power supply droop for low noise systems.

In addition, the logic's switching-current demand also requires bypass capacitors for each device, located as close to power or ground pin as possible. Usually a 0.1  $\mu$ F ceramic chip capacitor provides adequate decoupling. Including power supply decoupling at every step of the system design is critical for a high-performance, low-noise system. Power supply noise is easily coupled and radiated throughout the system.

Crosstalk is another system noise. If not addressed during system design, it can create problems in high-performance systems. Crosstalk refers to the noise created when a signal on an "active" trace is coupled onto an adjacent parallel "quiet" signal trace.

Forward crosstalk manifests itself as a negative voltage spike on the adjacent quiet trace and results from mutual inductance effects. Its amplitude and duration are generally much less than reverse crosstalk. Reverse crosstalk is

noise on the quiet trace resulting from a combination of capacitively-coupled and mutually-induced energy from the active signal trace. Its amplitude and duration are determined by the active signal's edge rate and the length of adjacent parallel traces. The faster the edge or the closer the adjacent traces, the higher the crosstalk amplitude. The longer the adjacent traces run, the longer the duration of the reverse crosstalk. Reverse crosstalk travels in the direction opposite to the active signal's propagation and lasts for twice the one-way delay time of the signal trace.

Crosstalk control methods include minimizing the coupled trace length and maximizing the distance between the two adjacent traces. If board area does not allow large spaces between lines, the insertion of a ground trace between the two adjacent traces also minimizes crosstalk.

Proper termination of all adjacent traces is important in minimizing crosstalk. Reflections are also propagating signals and will create crosstalk. Terminating adjacent transmission lines will eliminate the reflected signal.

Electromagnetic Interference (EMI) is another type of system noise. EMI is the radiation of energy outside the system. Whenever an electric charge is accelerated, electromagnetic waves result. The efficiency of this process is mainly determined by the geometry of the charge paths. The most significant charge paths in a system are the printed circuit board signal traces, power supplies, and I/O cables. The largest and most plentiful charge paths, they are also leading sources of EMI.

The EMI bandwidth is a function of the signal frequency, amplitude, edge rate, duty cycle, edge discontinuity, and ringing. These characteristics of high-performance logic, especially advanced CMOS logic, can cause signal traces and I/O cables to radiate more noise than ever before. The higher frequencies generated as a result of these characteristics will radiate more efficiently from signal lines because of their shorter wavelengths.

Addressing the characteristics of a signal that may create EMI is critical to reducing EMI, or achieving electromagnetic compatibility (EMC). Reliable solutions to EMC include proper shielding and grounding of all cables as well as proper termination of all signal traces. Adhering to other system design guidelines for power supply decoupling and crosstalk can also minimize EMI. Some of the output edge control techniques discussed later will also minimize EMI by directly effecting several key signal characteristics.

The last major form system noise is reflections on the transmission line and the resultant ringing. Ringing observed on signal traces has two sources: one is system-generated; the other, device-generated. The two are often confused. It is important to note that improperly terminated transmission lines will create ringing caused by reflections, i.e., system-generated noise.

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Reflections are caused by mismatches in impedance from driver to transmission line or from transmission line to receiver/termination. The magnitude of these reflections is related to the length of the transmission line and the impedance along the line. Transmission line impedances and driver/receiver I/O impedances seldom match.

Most often these impedances are orders of magnitude different. With the edge rates of today's advanced CMOS logic, transmission lines of approximately 20 centimeters (8 inches) or longer will most probably need some type of termination.

Choosing the right termination scheme is important. When designing with low-power advanced CMOS, do not select a termination that will dissipate several tens of milliamperes. Popular bipolar terminations such as a DC parallel termination (resistor to ground) or a Thevenin (voltage divider) termination (resistors to both rails) draw large amounts of DC current. Effective termination schemes that preserve low CMOS power consumption are a series resistor (for a single driver/receiver pair) or an AC parallel termination (resistor in series with a capacitor to ground) for distributed multiple loads.

Device-generated ringing is due to the parasitic LCR tank circuits in the IC and its load. The stimulus for this type of ringing is an overshoot or undershoot in the output signal. This ringing is minimized by slowing the output edge rate with higher loads or by improvements in IC circuitry.

#### WHAT IS DEVICE-GENERATED NOISE?

Device-generated noise includes dynamic threshold shift, ground bounce, and output undershoot.

The first type of device-generated noise is dynamic threshold shift. System designers are very familiar with DC input threshold requirements, namely  $V_{IH}$  (Input Voltage HIGH) and  $V_{IL}$  (Input Voltage LOW). For TTL-based logic, these levels are typically 2.0V and 0.8V, respectively. For CMOS-based logic, these levels are typically 70% and 30% of  $V_{DD}$ , respectively and are measured and guaranteed in a static (DC) mode only. Switching any part of the device-under-test is an invalid condition. In a real-life situation the IC is dynamic and so are the input thresholds.

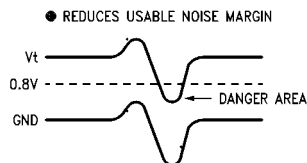


FIGURE 1. Dynamic Threshold

Dynamic input threshold shifts arise when one or several of the inputs are toggled, generating noise on the device's on-chip power rails. The input threshold voltage is proportional to the power supply voltage. Any fluctuation of these rails, such as ground bounce and/or undershoot, will create fluctuations of the input threshold. Figure 1 illustrates a negative excursion on the internal ground of an IC. The input threshold tracks this excursion and crosses through the static LOW input level. This creates an unwanted change of state on the output when the threshold falls below the input level. In this case, an undershoot caused by bounce on the chip ground causes a normally valid input level to create an invalid output state.

Dynamic threshold shifts may create problems on synchronizing inputs should the device's output noise be great

enough to cause the device's threshold voltage to shift across the input voltage level. On TTL-compatible inputs, dynamic threshold shifts could substantially reduce an already low noise margin.

In addition to causing erroneous changes in state, the output may begin to go into a high-frequency oscillation as input voltage levels approach the dynamic threshold. Regardless of whether the input in question is a synchronizing input, this high frequency oscillation will increase chip heating. Should this situation continue, device reliability could be effected.

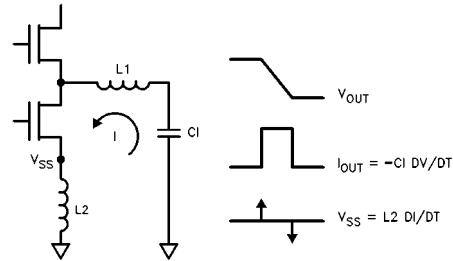


FIGURE 2. Ground Bounce Model

The second type of device-generated noise is ground bounce or simultaneous switching noise. Ground bounce or  $V_{OLP}$  (Voltage Output LOW, Peak) and undershoot or  $V_{OLV}$  (Voltage Output LOW, Valley) are names given to noise levels associated with the output of a logic device. While these two issues are not new to logic, they are of greater concern with advanced logic families. Since advanced CMOS outputs switch rail to rail at high speed and into heavy loads, performance and design concerns have risen in this area.

Similarly,  $V_{DD}$  droop and overshoot are also device-generated noise issues. However, since both affect the logic HIGH level and since using CMOS outputs to drive TTL inputs provides much higher noise margin than the logic LOW level, this discussion focuses on low-level noise margin issues.

As the model in Figure 2 illustrates, ground bounce is the voltage induced on the device ground inductance by current as it quickly discharges from a capacitive load, sinking into the output's N-channel transistor. The greater the amount and rate of discharge that is created by multiple simultaneously switching outputs, the greater the ground bounce level. Essentially there are more current sources sinking current into the same ground inductor.

Device undershoot or  $V_{OLV}$  (Voltage Output LOW, Valley) is simply a function of the LCR tank circuit at the output. As edge rates increase, undershoot and subsequent ringing increase. Undershoot also decreases as the capacitive load on the output increase and/or as the inductance of the output decreases. Therefore, advanced CMOS logic devices driving one or two other advanced CMOS logic devices will have more undershoot than an advanced CMOS device driving a heavily loaded bus. For this reason, in most systems undershoot levels are much less than those observed in test fixture environments. Also, improper bus termination may appear to worsen undershoot. In fact it is the energy of the reflected wave that increases the undershoot and not the device itself. Most undershoot levels in excess of 2.0V are the result of some mismatched impedance along the transmission line and can be eliminated with proper termination.

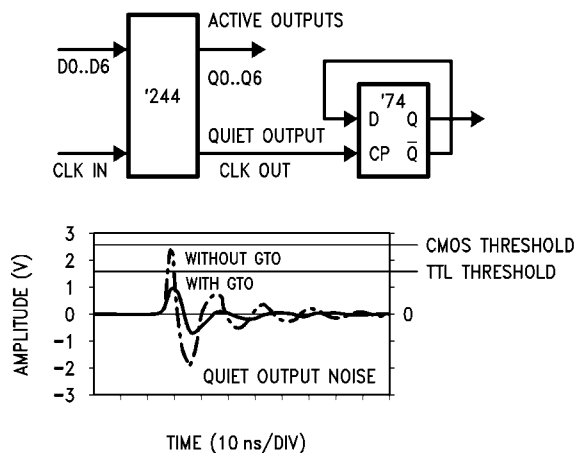


FIGURE 3. Example of Ground Bounce

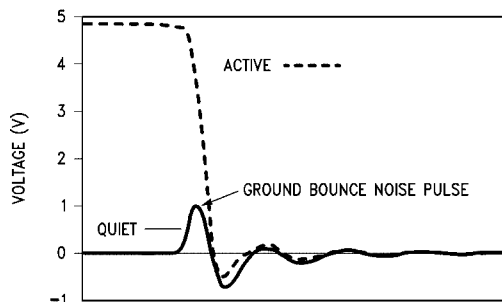


FIGURE 4. Location of Bounce Pulse

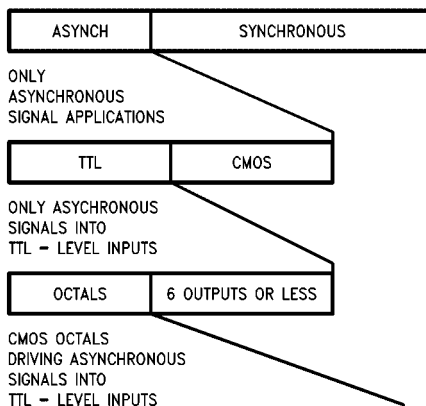


FIGURE 5. Application Segments

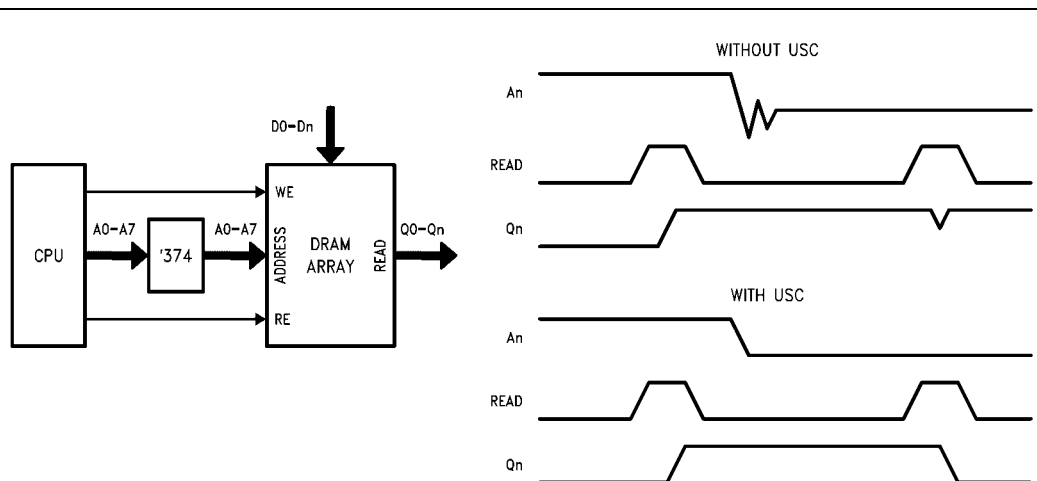


FIGURE 6. Example of Undershoot

#### WHERE CAN DEVICE-GENERATED NOISE AFFECT SYSTEM PERFORMANCE?

An integrated circuit ground inductor's  $di/dt$  is determined by the number of outputs switching and the capacitive load on each output. In a system, transmission line effects will reduce the effective capacitive load the output may actually drive. In a test fixture, the load is made up of low-dissipation factor chip capacitors soldered directly to the output pins. In a system, a finite physical distance separates the various capacitive loads from each other as well as the driver's output. The net effect of capacitance distributed along the transmission line is to lower the effective impedance of the transmission line. As a result, ground bounce in a system is typically 50% less than test fixture measurements. Test fixture measurements of ground bounce should only be used for comparative analysis and characterization.

The magnitude of system ground bounce and the segment of applications where that bounce may present problems is very small. Ground bounce occurs concurrently with the transition of the active outputs of the device. Ground bounce on quiet output(s) driving synchronous signals—such as data and address lines—are not of concern since these signals will not be synchronized or sampled until long after ground bounce has settled out. See Figure 4.

However, while asynchronous signals, such as resets, pre-sets, latch enables, and clock lines, typically number far fewer than synchronous signals in a system they may be more susceptible to ground bounce.

Since substantial ground bounce voltage levels are only achieved with six or more outputs switching simultaneously in the same package, device with eight or more bits, i.e., octals, are the primary focus of ground bounce.

Also, noise signals, such as ground bounce, driven into CMOS-level inputs generally have no effect due to the higher amount of energy needed to switch CMOS inputs. Typical voltage levels needed to switch full CMOS inputs are 3.0V for approximately 2.0 ns; ground bounce levels in

a system or a test fixture do not reach this level. However, ground bounce on asynchronous signals into TTL-input levels may cause system errors. Typically TTL inputs need only 1.7V of noise of 2.0 ns to switch (e.g. FAST® and ALS).

For these reasons, the small segment of applications where ground bounce noise may compound with system noise levels and possibly affect system performance is where advanced CMOS octals drive asynchronous signals into TTL-level inputs. See Figure 5. Since the mechanisms are similar, shifts in dynamic threshold are also a possible concern in this small segment.

Undershoot, either on quiescent low or HIGH-to-LOW switching outputs, can create noise problems in some systems by generating excess ringing on the signal line. As stated earlier, ringing also adds to EMI and crosstalk noise. Additionally, most devices driven by logic devices have clamp diodes on their inputs that will limit the input voltage excursions. However, as devices such as DRAMs, DACs, and PLDs have no protection and are sensitive to negative voltage excursions on the input, system faults or damage to these devices, caused by latch-up, may result. The use of series resistors can safeguard against such faults.

The system designer may further minimize ground bounce and undershoot effects by choosing surface mount technology (SMT). SMT package inductance on the order of 2 nH to 4 nH can reduce ground bounce and undershoot by as much as 25%, without the board area penalty incurred by larger non-standard pinout. Also, if the design allows, placing asynchronous signal lines on pins closest to the ground pin will minimize the noise on these lines—as much as 20% less noise than pins furthest from ground.

If device-generated noise is still a critical issue in the system design, Fairchild Semiconductor Corporation has implemented several design improvements that greatly minimize device-generated noise. The result is an extension to the FACT™ line—FACT Quiet Series or FACT QS.

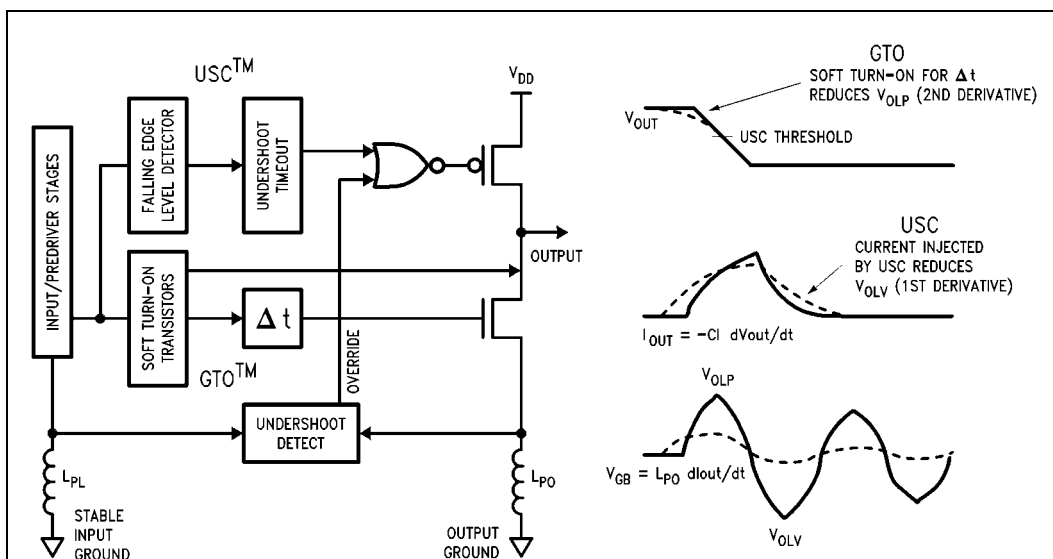


FIGURE 7. Fairchild Semiconductor's Proprietary Noise Control Circuitry

#### DESIGN INNOVATIONS RESOLVE DEVICE NOISE ISSUES

FACT Quiet Series implements patented technological breakthroughs in device-generated noise suppression as well as several major performance improvements. Design improvements include a graduated output N-channel turn-on circuit, and an output undershoot correction circuit.

A graduated output N-channel turn-on circuit (GTO™), greatly reduces ground bounce. As Figure 2 illustrated, ground bounce is a function of the output waveshape,  $d^2v/dt^2$ . Reducing package and chip inductance does have some effect in reducing ground bounce, but the reduction in ground bounce is not linear with inductance reduction. Package inductances may change by an order of magnitude, yet ground bounce is reduced only by as much as 25%.

Second order effects, such as increases in  $di/dt$  as output reactance is decreased, cause ground bounce reductions to flatten as inductance is reduced. The cost of reducing inductance on dual-in-line packages is an increased number of power and ground pins, increased package size, and a non-standard pinout. Package pinout changes have negligible effect on surface mount devices where inductance is LOW to begin with.

The greater reduction in ground bounce is found by rounding the transition point on the HIGH-to-LOW edge, or waveshaping. Figure 7 illustrates the effect of output waveshaping on ground bounce. This waveshaping is actually achieved by combining several design techniques. The two most notable are the slow decay of the load capacitance charge through a soft turn-on circuit prior to the actual transition, and the delaying of the actual turn-on of the large N-channel output transistor.

Since ground bounce levels are more substantial on the HIGH-to-LOW transition, the LOW-to-HIGH transition remains unchanged. In addition, design considerations were taken to ensure the integrity of the HIGH-to-LOW edge rate, and thereby maintain device AC performance.

Ground bounce on advanced CMOS logic without output waveshaping is on the order of 2.0V to 3.0V  $V_{OLP}$  in a test fixture environment. In the same environment, FACT QS, with the GTO circuitry, provides  $V_{OLP}$  performance in the range of 1.0V to 1.3V. In a system, 30% to 50% lower  $V_{OLPs}$  should result.

Another design improvement, undershoot corrector circuitry (USC), reduces output undershoot, both on the switching and quiescent (at ground) outputs. Undershoot is also a matter of  $di/dt$ . As output edge rates speed up and voltage swings increase, undershoot increases. Undershoot also increases as the number of simultaneously switching outputs increases. The result,  $V_{OLV}$ , can be seen on both the switching edges as well as outputs quiescent at ground.

The undershoot correction circuit works by limiting negative  $di/dt$  excursions. The first part of this two-stage circuit senses a HIGH-to-LOW edge. At a predetermined point on that edge, the undershoot corrector is turned on. The corrector simply activates a P-channel transistor which sources current into the output. This softens the  $di/dt$  that occurs when the load is depleted of charge. An internal RC timer controls the duration and decay of the correction.

Should the RC timer time out before undershoot is fully resolved, a differential amplifier, sensing that the output voltage is still below the input ground, keeps the current source turned on. This two-stage design is more reliable because of the time required for the current injector to turn on after the output goes negative.

Because USC operation is affected by package inductance, plastic DIP packages react differently than ceramic DIP packages. Similarly, surface mount devices have a different correction level. As ground bounce and undershoot decrease with decreasing inductance, the need for undershoot correction also decreases with decreasing inductance.

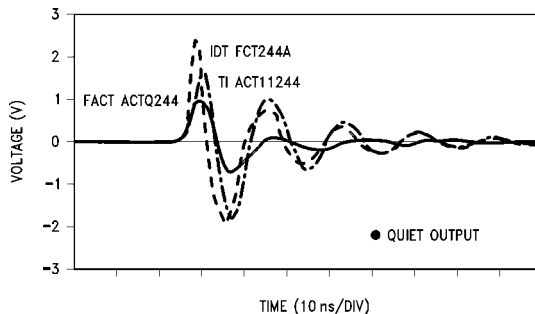


FIGURE 8. AC MOS Comparison

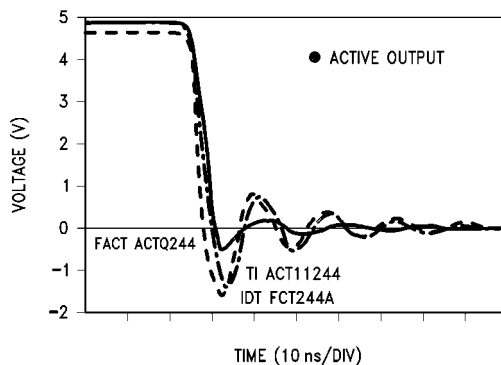


FIGURE 9. AC MOS Comparison

#### OUTPUT CONTROL CIRCUITRY RESULTS IN LOWER NOISE

Figure 8 and Figure 9 compare three major AC MOS product lines. These AC MOS manufacturers have different levels of noise suppression. All measurements were taken using an industry-accepted fixture and methodology.

FACT QS is manufactured on a smaller geometry CMOS process than standard FACT products. Because of the use of this technology, FACT QS AC speeds are faster than standard FACT. Propagation delays as well as set-up and hold times are also specified identically to or faster than standard FACT.

#### DESIGN IMPROVEMENTS GO BEYOND NOISE

In addition to improvements which reduce device-generated noise, FACT QS also incorporates design improvements for greatly enhanced performance and reliability. These parameters include specification of output pin-to-pin propagation delay skew, higher electrostatic discharge (ESD) immunity, and higher latchup immunity, than standard FACT products.

Pin-to-pin skew becomes an issue as high-performance logic is designed into clock distribution and other timing-sensitive applications. Since, part-to-part skews are not effected by variations in  $V_{DD}$  or temperature, the only variable that could effect part-to-part skew is processing variations from one device to another. Part-to-part skews may be interpreted by subtracting the 25°C, 5.0V -  $V_{DD}$  propagation delay minimum specification from the maximum specification on most advanced CMOS logic data sheets.

Guaranteed AC MOS logic pin-to-pin skew specifications are unique to Fairchild Semiconductor's FACT QS product

line. For clock distribution applications where all outputs transition to the same state simultaneously, output skew is typically less than 500 ps, with worst case being 1.0 ns. For bus applications where outputs can transition to either state simultaneously, typical skew is less than 800 ps, with worst case being 1.0 ns.

Another performance improvement is higher ESD immunity. Process improvements for FACT QS have improved ESD immunity to 8,000V or better. ESD is specified at 6,000V typical, with worst case being at 4,000V minimum.

A third performance improvement in Fairchild's FACT QS is a higher latch-up immunity specification. As with standard FACT, the implementation of epitaxial silicon in the FACT process essentially eliminated latch-up possibility. The currents needed to latch-up devices manufactured on the FACT processes are typically in excess of 1A. FACT QS latchup immunity is tested to 300 mA on the inputs and up to 1A on the outputs. Latchup immunity is specified at 300 mA minimum at +125°C.

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