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Limiting Cross-Conduction Current in Synchronous Buck Converter Designs

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Introduction

The synchronous buck converter is the topology of choice for PC and notebook computers. The reason for this favored status is that this topology offers designers an ease of control, a small footprint and high power conversion efficiencies at a relatively low cost. An important consideration in designing this synchronous buck converter is limiting the shoot-through or cross conduction current. Through mathematical analysis, MOSFET designers and power supply designers test the suitability of a specific device for its use as a synchronous rectifier in the converter.

What this Application Note Will Do

- Explore several solutions that consider inductances involved in this design to better understand this complex phenomenon
- Demonstrate how the gate inductance tends to make the cross conduction current or shoot through worse
- Demonstrate how source inductance helps to keep the gate source voltage at a lower level
- Present the equations that describe the gate voltage in time as a function of all the circuit parameters

The Importance of Choosing the Right MOSFET

Shoot-through can be understood by examining the factors that control the induced gate-source voltage when the drain voltage is switched between near ground and input voltage levels. This situation is encountered in the synchronous buck topology during the time interval when the top MOSFET is switched on while the gate driver holds the lower MOSFET off.

If the induced voltage is larger than the gate threshold voltage of the LS MOSFET, it could be turned ON while the top MOSFET is ON, leading to excessive power dissipation in both MOSFETs and ultimately, lead to failure in either one or both devices. By examining the mechanism causing this phenomenon, proper MOSFET selection can be made and cross conduction can be eliminated or avoided.

Simplified Shoot-Through in the Synchronous Buck Converter

The first example is the simple equivalent circuit in Figure 1 where no parasitic inductances are considered. Our analysis addresses only the transition time when the HS MOSFET

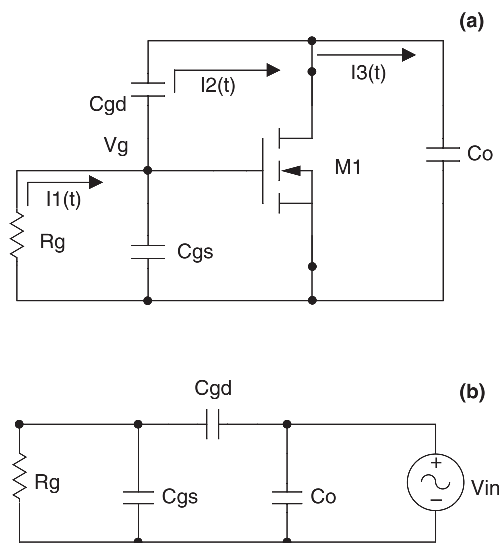


Figure 1. Schematic and equivalent circuit used for analysis

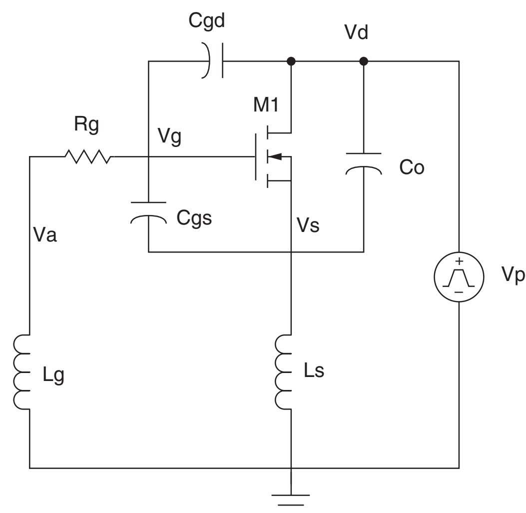


Figure 2. Schematic used in equation derivation with source and gate inductance

turns on while the LS MOSFET is being held off by the action of the gate driver. The HS MOSFET does not experience shoot-through when it is turned off.

The gate voltage rise of the LS MOSFET will be determined by the rate of change on the drain voltage as well as the MOSFET's gate-source capacitance (Cgs) and the drain-source capacitance (Cgd) and the effective series gate resistance. The effective series resistance is calculated from the driver output resistance and the MOSFET's internal effective gate equivalent series resistance (ESR) Rg.

The Analysis

Figure 1 shows the LS MOSFET in the off state and its equivalent circuit for this analysis. This can be calculated by writing Kirchoff's equations for the equivalent circuit of the lower MOSFET Fig. 1(b). Vin is a voltage source representing the effect of the external circuit as the top MOSFET turns ON.

The Drain Voltage = Vin = a*t, where "a" is the rate of change of the drain voltage and "t" is Time. Kirchoff's equation for this circuit yields:

$$\mathrm{Vin} := \int \frac{i3(t)}{Co}dt - \int \frac{i2(t)}{Co}dt$$

$$a \bullet t := \int \frac{i3(t)}{Co}dt - \int \frac{i2(t)}{Co}dt$$

$$\frac{d}{dt}(a \bullet t) := \frac{1}{Co} \bullet (i3(t) - i2(t)) \tag{1}$$

Similarly,

$$i2(t) \bullet \left(\frac{1}{Co} + \frac{1}{Cgd} + \frac{1}{Cgs}\right) - \frac{i3(t)}{Co} - \frac{il(t)}{Cgs} = 0 \tag{2}$$

$$Rg \bullet il(t) + \int \frac{i1(t)}{Cgs}dt - \int \frac{i2(t)}{Cgs}dt$$

$$\frac{d}{dt}(Rg \bullet il(t)) + \frac{i1(t)}{Cgs} + \frac{i2(t)}{Cgs} = 0 \tag{3}$$

Solving equations (1), (2) and (3) provides the value of current through the gate resistor:

$$i1(t) := a\,Cgd\left(1 - e^{\left(-\frac{t}{Rg(Cgs + Cgd)}\right)}\right)$$

The Gate Voltage = vg(t) = Rg*i1(t) is calculated by:

$$Vg(t) := a\,Rg\,Cgd\left(1 - e^{\left(-\frac{t}{Rg(Cgs + Cgd)}\right)}\right) \tag{4}$$

The condition for no shoot-through in a given MOSFET under a given rate of change of the drain voltage "a" can be calculated using equation (4).

At the end of the rise time, t = Tr and Vcc = Input Voltage (12V-19V). At this instance, if Vg(t) ≥ Vgth (the MOSFET gate threshold voltage) cross conduction occurs. To find the value for the parameter "a" to cause cross conduction, equation (4) must be solved by substituting

$t = Tr = \frac{Vcc}{a}$ in (4):

$$VgatTr := a\,Rg\,Cgd\left(1 - e^{\left(-\frac{Vcc}{a\,Rg(Cgs + Cgd)}\right)}\right) \tag{5}$$

The solution for the maximum value of "a" in equation (5) may be obtained by using a suitable numerical solve function typically found in analysis tools such as in Maple™.

The Critical Point

The plot of the gate voltage, Vg, versus the value "a" and Rg is shown in Figure 4.

The intersection of this curve with the line Vg = Vgth determines the minimum value of a_{crit} where cross conduction occurs.

Note that in Figure 4 Vg approaches an asymptotic value as "a" approaches ∞. This allows additional simplification of the analysis.

For equation (5) let us get the limit of Vg(t) as "a" approaches ∞,

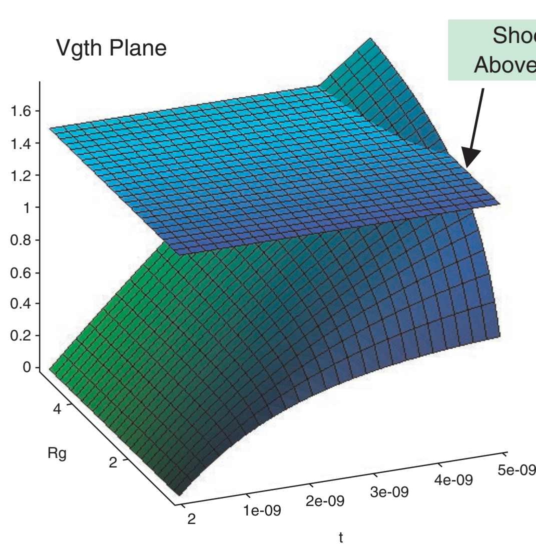
$$\lim_{a \to \infty} a\,Rg\,Cgd\left(1 - e^{\left(-\frac{Vcc}{a\,Rg(Cgs + Cgd)}\right)}\right) = \frac{Vcc\,Cgd}{Cgs + Cgd}$$

At a = ∞ we get $Vg = \frac{Cgd\,Vcc}{Cgs + Cgd}$ (6)

Where Vg is the gate voltage at the asymptotic condition of "a" approaching ∞.

At this point, the conditions for cross conduction can be evaluated as follows, If Vg calculated from equation (6) is less than the lower MOSFET gate threshold voltage Vgth i.e. Vg < Vgth, then no cross conduction is expected. Notice that Vg in (6) is independent of Rg, which is to be expected. As "a" gets larger, the impedance of Cgs becomes much smaller than Rg and it becomes the only determining factor, since both Rg and Cgs are connected in parallel. Alternatively, if Vg > Vgth, then cross conduction can be expected at some value of "a".

Even if a MOSFET meets the condition Vg ≥ Vgth in equation (6), it still may be suitable for the application as a synchronous rectifier as long as it satisfies equation (5) for an actual circuit rise time with a finite value of "a".



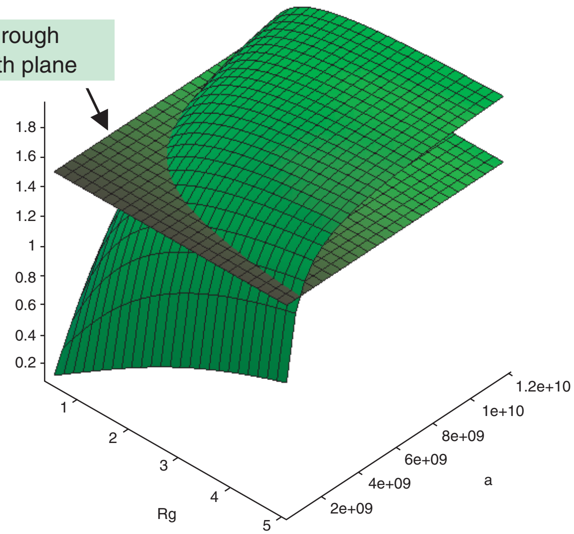


Figure 3. The gate voltage, Vg, plotted against Rg and Time t and the Vgth level of 1.5V

Figure 4. The gate voltage as a function of a and Rg and the Vgth level of 1.5V

Shoot through analysis with considerations for parasitic gate and source inductances

Now let us examine the shoot through phenomenon when we include both the Source and gate inductances in the circuit as in Figure 2. In order to fully understand the mechanics of shoot through under these conditions, the equations are calculated below under several conditions of input voltage. In the first case, only the rising edge of Vp is considered and the equations are solved accordingly.

Let's write the equations for Figure 2 are as follows:

$$Vd(t) := \frac{Vm\ t}{tr}$$

$$e1 := Id(t) + Co\left(\frac{Vm}{tr} - \left(\frac{d}{dt}Vs(t)\right)\right) + Cgd\left(\frac{Vm}{tr} - \left(\frac{d}{dt}Vg(t)\right)\right) = 0$$

$$e2 := Co\left(\frac{d^2}{dt^2}Vs(t)\right) + Cgs\left(\left(\frac{d^2}{dt^2}Vs(t)\right) - \left(\frac{d^2}{dt^2}Vg(t)\right)\right) + \frac{Vs(t)}{Ls} = 0$$

$$e3 := \frac{Vg(t) - Va(t)}{Rg} + Cgs\left(\left(\frac{d}{dt}Vg(t)\right) - \left(\frac{d}{dt}Vs(t)\right)\right) + Cgd\left(\left(\frac{d}{dt}Vg(t)\right) - \frac{Vm}{tr}\right) = 0$$

$$e4 := \frac{Va(t)}{Lg} + \frac{\left(\frac{d}{dt}Va(t)\right) - \left(\frac{d}{dt}Vg(t)\right)}{Rg} = 0$$

Where:

Vm = Maximum Gate Drive voltage
Cgs = Gate to Source capacitance
Co = Drain to Source capacitance
Lg = Total Gate inductance
tr = Driving voltage rise time
Cgd = Gate to Drain capacitance
Rg = Total Gate series resistance
Ls = Total Source inductance

The gate drive voltage is a linear ramp with respect to time t.

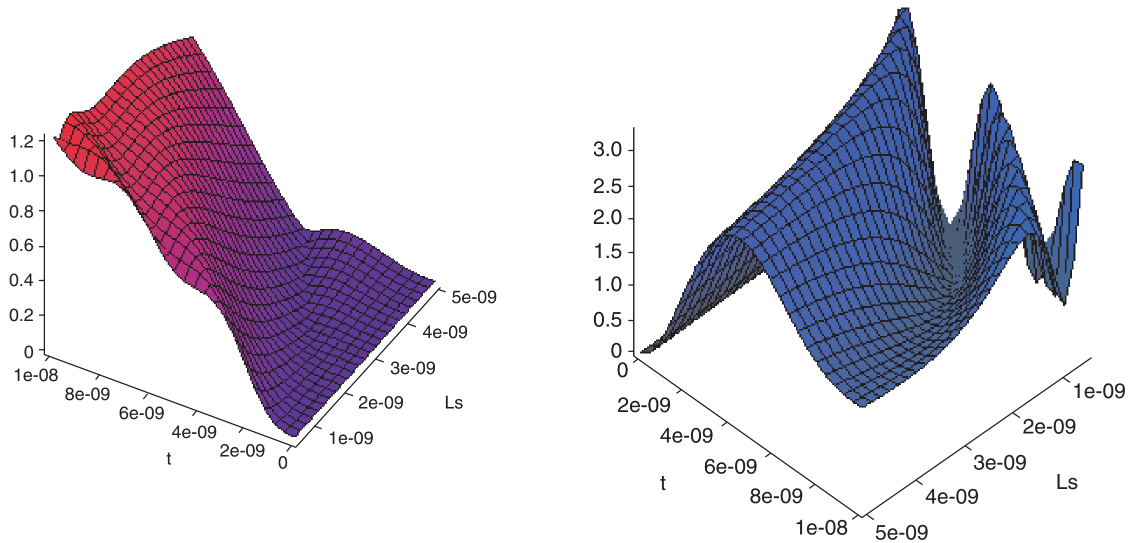


Figure 5. Gate voltage (left) and current in the driving source Vp (right). tr = 10nS

By solving the differential equations e1…e4 above, this results in getting all the node voltages as a function of time t. Unfortunately the resulting equations are too long and complex to fully visualize so in order to fully understand the effects of both the source inductance Ls and the gate inductance Lg, we can generate few of graphs using these equations to show us the trends.

Figure 5 (left) shows the shoot through gate voltage for a rise time of 10nS and a total drain voltage transient of 19 Volt. This level is quite realistic and agrees with lab results very well. Fig 5 (right) is the current in the driving voltage Vp. This is the current that usually flows in the high side MOSFET while turning on adding one further component to the dynamic losses and requires that the gate driver IC can sink this much current without any significant rise in voltage.

The situation is much more complicated when we drive the low side MOSFET with a 19V at a rise time of 1nS. As can be seen from Figure 6, the current that flows in Co also flows in Ls adding one more complexity to the solution since this current tends to be beneficial from the shoot through point of view since it tends to raise the source voltage resulting in lower gate-source voltage and hence causing no shoot through. In fact, under the right conditions of Ls and Lg, we may get a negative Gate-Source voltage completely blocking any chance of the MOSFET turning on as can be seen in Figure 7.

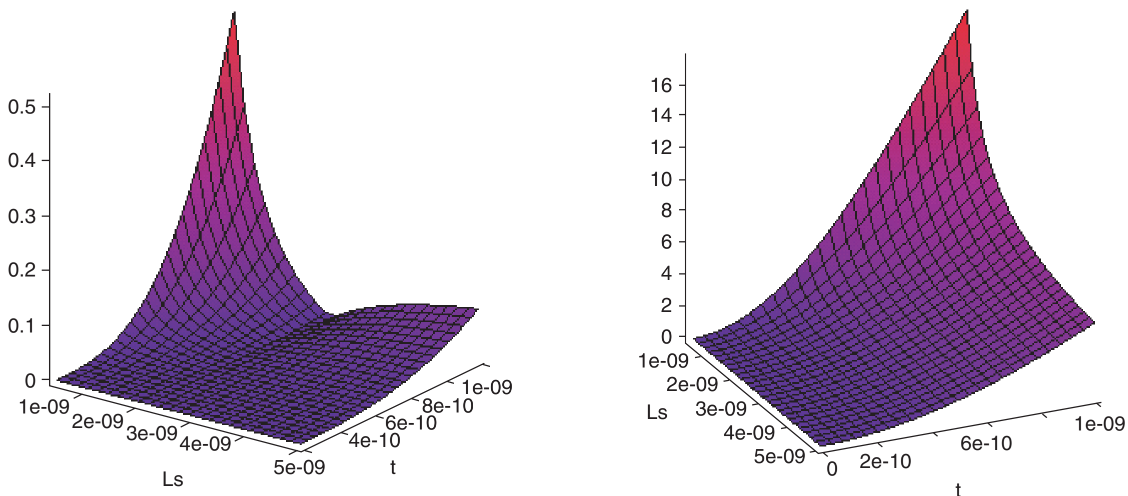


Figure 6. Gate-source voltage (left) and current in the driving source (right) Vp. tr = 1nS

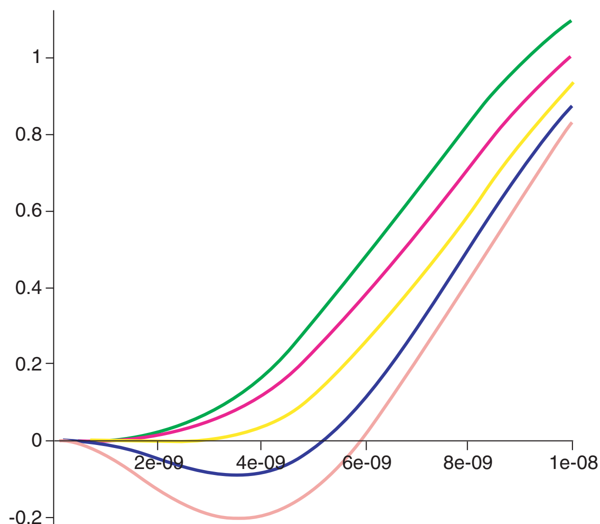


Figure 7. Gate-Source voltage at different combinations of Lg and Ls. Notice the Blue and Red plots going negative for part of the cycle

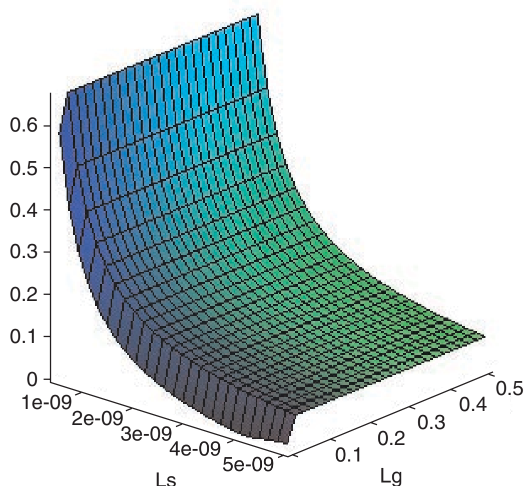


Figure 8. Gate voltage as a function of Gate inductance Lg and Source inductance Ls. tr = 1nS

Figure 6 (left) represents the gate-source voltage when the rise time is 1nS. This transition time is very close to the current high performance circuit conditions where 3nS–5nS is encountered on a regular basis. Within the next few years, sub nanosecond transitions will be the norm in high performance DC-DC power supplies. Notice that the shoot through gate-source voltage is much smaller than in the 10nS rise time case because of the effect of Co on the current flowing in the source inductance Ls. On the other hand Figure 6 (right) represents the current in the driving voltage Vp that, as we said before, flows normally in the high side MOSFET. This means that the gate driver needs to be designed to sink up to 16 amps of peak current, a sobering fact for their designers. The same 16 Amp will flow in the HS MOSFET adding significant amount of losses to the MOSFET's turn on losses. This is clearly is an undesirable side effect since a very low source inductance is desirable for fast turn on/off. As it is always the case with any engineering problem, a compromise between all of these effects must be reached and in order to do this, one must fully understand the underlying issues and problems and use this knowledge for the best results.

Now that we understand the shoot through phenomenon with the inclusion of both Lg and Ls, we need to understand the relative influence of each of these parasitic inductances. Figure 8 shows the shoot through gate-source voltage as a function of Lg and Ls at the end of the rise time of 1nS. It can be clearly seen that except for very low Lg < 1nH, the gate-source voltage is dominated by the source inductance Ls where the larger Ls is the smaller the gate-source voltage and the less possibility of the shoot through occurring.

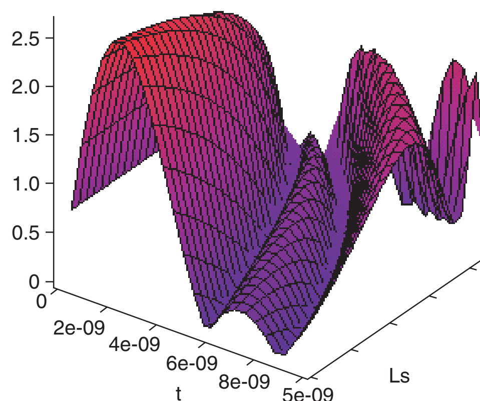


Figure 9. Gate to ground voltage for wide pulse. tr = 10nS

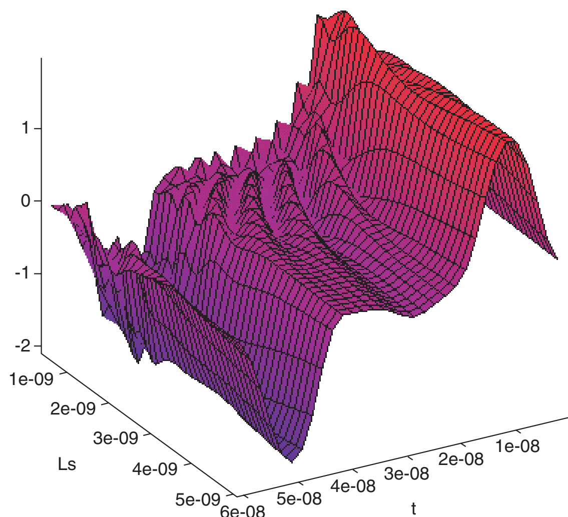


Figure 10. Gate to source voltage for wide pulse. tr = 10nS

To further understand the this phenomenon, we derived a solution with a single 19 volt pulse introduced to the gate terminal, Figures 9 and 10 are the gate-ground and gate-source voltages. Figure 10 shows the negative voltage swing

when the HS MOSFET turns off causing no shoot through. Figure 9 shows the gate-ground voltage in the case of 10nS rise time. When compared to Figure 5 (left) showing the gate-source voltage under identical conditions, it becomes evident that measuring the gate-ground voltage of 2.5 Volt and predicting the existence of shoot through based on the fact that the gate-ground voltage is larger than the gate threshold voltage (Vgth) is incorrect since Figure 5 (left) clearly indicates that the Gate - Source voltage is about 1.2 Volt only and hence for a MOSFET with Minimum Vgth of say 1.5 Volt there will be no shoot through though the external observation of the gate-ground voltage is 2.5Volt.

Figure 11 depicts the gate-source voltage with a rise time of 1nS using the circuit in Figure 2 with both Lg and Ls present. The graph shows that for equal silicon parameters shoot through is likely to take place in the device with the lowest Ls package but unfortunately that means that the dynamic losses in the package with the high Ls will be higher.

Figure 11 shows the complexity of gate-source voltage waveform as Ls varies from 0.5nH to 5nH.

For completion Figure 12 shows the complete equivalent circuit of the LS MOSFET on the left and on the right the solution of all three different cases 1–The simple solution, 2–with the addition of Ls&Lg, 3–with the addition of Ls and Lg and all inter-electrode ESR.

Further Work

One of the facts about the gate ESR (Rg) is that it is a distributed resistance on the MOSFET die. This means that depending on a region's position the effective Rg is different from one region to the other leading to some regions bearing the full brunt of the shoot through losses while other regions will have no shoot through losses at all. Theoretical mathematical and simulation work shows that this is the case.

Conclusion

1. Equation (5) should be used to evaluate a given MOSFET susceptibility to shoot-through for almost all applications today. Equation (8) should be used for the projected applications of the next few years where the rise and fall times are in the sub nanosecond range.

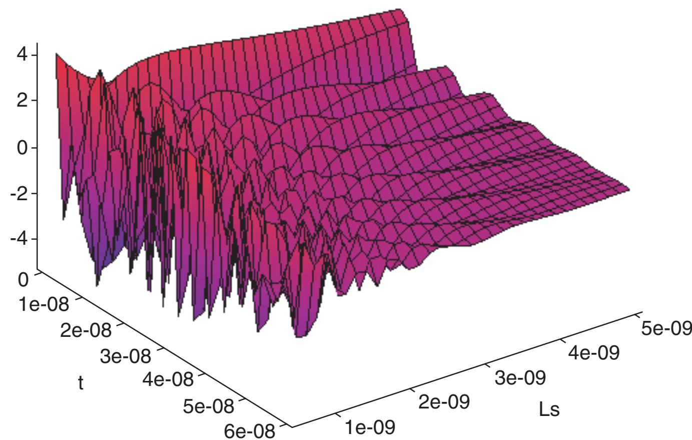
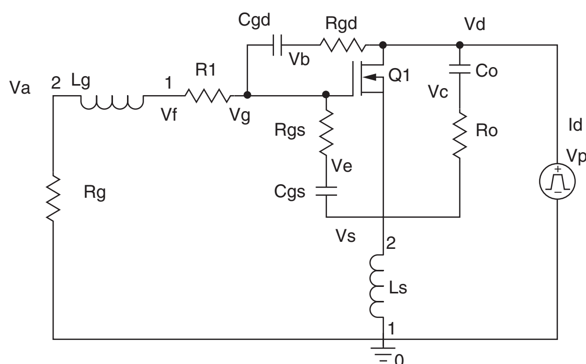


Figure 11. Gate to Source voltage for a very narrow pulse. tr = 1nS



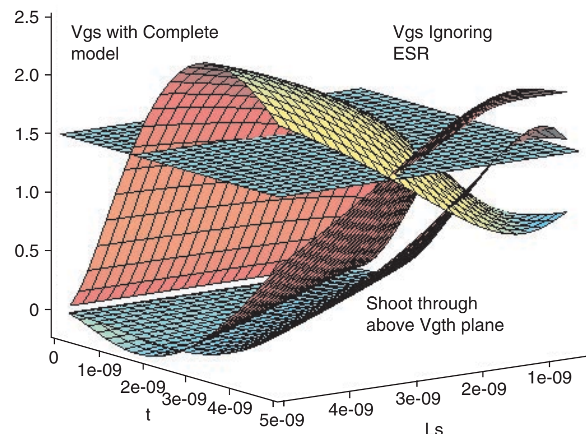


Figure 12. Complete equivalent circuit including inter-electrode ESR

1. The gate-ground voltage alone does not tell whether shoot through will take place or not but rather the gate-source voltage is the decisive factor. Although this conclusion is very obvious, it is not observable in the lab since the source of the synchronous rectifier is always connected to ground; gate-ground voltage is usually measured since it is the only available measurement. I have to say that I have been guilty of this practice before this work.

2. Source inductance plays a more pronounced role in determining whether shoot through occurs or not mainly due to the effect of Co and Ls.

3. A thorough and complete understanding of the parasitic inductances of all our packages is mandatory to evaluate the susceptibility of a given MOSFET in a given package to shoot through in preparation for the sub 1nS switching of the future.

4. Combining the shoot through loss mechanism with Reverse recovery loss mechanism, it becomes obvious that some loop inductance is mandatory to mitigate the switching losses. Exactly how much inductance is needed depends on the circuit and the individual MOSFETs and gate drivers utilized in the application.

5. There is a large current component that the high side MOSFET has to deliver to charge all the inter-electrode capacitors. This current is dependant on the rise time of the voltage of the junction between the high side and the low side MOSFETs and may become the dominant switched current in the high side MOSFET for rise times of <1nS.

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